ACS
(Al's Circuit Simulator)
Users manual

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Contents

Chapter 1

Introduction

1.1 What is it?

ACS is a general purpose mixed analog and digital circuit simulator. It performs nonlinear dc and transient analyses, fourier analysis, and ac analysis linearized at an operating point. It is fully interactive and command driven. It can also be run in batch mode. The output is produced as it simulates. Spice compatible models for the MOSFET (levels 1-6) and diode are included in this release.

Since it is fully interactive, it is possible to make changes and re-simulate quickly. This makes ACS ideal for experimenting with circuits as you might do in an iterative design or testing design principles as you might do in a course on circuits.

In batch mode it is mostly Spice compatible, so it is often possible to use the same file for both ACS and Spice.

The analog simulation is based on traditional nodal analysis with iteration by Newton's method and LU decomposition. An event queue and incremental matrix update speed up the solution considerably for large circuits and provide some of the benefits of relaxation methods but without the drawbacks.

It also has digital devices for true mixed mode simulation. The digital devices may be implemented as either analog subcircuits or as true digital models. The simulator will automatically determine which to use. Networks of digital devices are simulated as digital, with no conversions to analog between gates. This results in digital circuits being simulated faster than on a typical analog simulator, even with behavioral models.

ACS also has a simple behavioral modeling language that allows simple behavioral descriptions of most components including capacitors and inductors.

ACS is an ongoing research project. It is being released in a preliminary phase in hopes that it will be useful and that others will use it as a thrust or base for their research.

1.2 Starting

To run this program, type and enter the command: `acs`, from the command shell.

The prompt `-->` shows that the program is in the command mode. You should enter a command. Normally, the first command will be to `build` a circuit, or to `get` one from the disk. First time users should turn to the examples section for further assistance. There is a `help` command, in case you get lost.

To run in batch mode, use `acs` *`file`*. This will run the *file* in batch mode. If it ends with an `.end` command, it will exit when done, otherwise it will revert to command mode.

1.3 How to use this manual

The best approach is to read this chapter, then read the command summary at the beginning of chapter 2, then run the examples in the tutorial section. Later, when you want to use the advanced features, go back for more detail.

This manual is designed as a reference for users who are familiar with circuit design, and therefore does not present information on circuit design but only on the use of this program to analyze such a design. Likewise, it is not a text in modeling, although the models section does touch on it.

Throughout this manual, the following notation conventions are used:

- `Typewriter` font represents exactly what you type, or computer output.
- `Underlined typewriter` font is what you type, in a dialogue with the computer.
- Command words are shown in mixed UPPER and lower case. The upper case part must be entered exactly. The lower case part is optional, but if included must be spelled correctly.
- *Italics* indicate that you should substitute the appropriate name or value.
- Braces { } indicate optional parameters.
- Ellipses (...) indicate that an entry may be repeated as many times as needed or desired.

1.4 Command structure

Commands are whole words, but usually you only have to type enough of the word to make it unique. The first three letters will almost always work. In some cases less will do. The whole word is significant, if used, and must be spelled correctly.

In files, commands must be prefixed with a dot (.). This is done for compatibility with other simulation programs, such as SPICE.

Command options should be separated by commas or spaces. In some cases, the commas or spaces are not necessary, but it is good practice to use them.

Upper and lower case are usually the same.

Usually options can be entered in any order. The exceptions to this are numeric parameters, where the order determines their meaning, and command-like parameters, where they are executed in order. If parameters conflict, the last takes precedence.

In general, standard numeric parameters, such as sweep limits, must be entered first, before any options.

Any line starting with `*` is considered a comment line, and is ignored. Anything on any line following a quote is ignored. This is mainly intended for files.

This program supports abbreviated notation for floating point numeric entries. 'K' means kilo, or 'e3', etc. 'M' and 'm' mean milli, not mega (for Spice compatibility). 'Meg' means mega. Of course, it will also take the standard scientific notation. Letters following values, without spaces, are ignored.

T = Tera = e12
G = Giga = e9
Meg = Mega = e6
K = Kilo = e3
m = milli = e-3
u = micro = e-6
n = nano = e-9
p = pico = e-12
f = femto = e-15

1.5 Standard options

There are several options that are used in many commands that have a consistent meaning.

`Quiet` Suppress all unnecessary output, such as intermediate results, disk reads, activity indicators.

`Echo` Echo all disk reads to the console, as read from the disk.

`Basic` Format the output for compatibility with other software with primitive input parsers, such as C's *scanf* and Basic's *input* statements. It forces exponential notation, instead of our standard abbreviated notation. Any numbers that would ordinarily be printed without an exponent are not changed.

`Pack` Remove extra spaces from the output to save space at the expense of readability.

`<` Take the input from a file. The file name follows in the same line.

`>` Direct the output to a file. The file name follows. If the file already exists, it will ask permission to delete the old one and replace it with a new one with the same name.

`>>` Direct the output to a file. If the file already exists, the new data is appended to it.

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Chapter 2

Command descriptions

2.1 Command Summary

`*` Comment line.

`!` Pass a command to the operating system.

`<` Batch mode.

`>` Direct the "standard output" to a file.

`AC` Performs a small signal AC (frequency domain) analysis. Sweeps frequency.

`ALARM` Select points in circuit check against limits.

`ALTER` Perform analyses in queue. Changes follow. (Not implemented.)

`BUILD` Build a new circuit or change an existing one.

`CHDIR` Change current directory.

`CLEAR` Delete the entire circuit, titles, etc.

`DC` Performs a nonlinear DC analysis, for determining transfer characteristics. Sweeps DC input or component values.

`DELETE` Delete a part, or group of parts.

`DISTO` SPICE command not implemented.

`EDIT` Edit the circuit description using your editor.

`END` Perform analyses in queue. New circuit follows. (Implemented incorrectly.)

`EXIT` Exits the program. (Same as quit)

`FANOUT` List by node number, the branches that connect to each node.

`FAULT` Temporarily change a component.

`FOURIER` Transient analysis, with results in frequency domain. (Different from SPICE.)

`GENERATOR` View and set the transient analysis function generator.

`GET` Get a circuit from a disk file. Deletes old one first.

`IC` Set transient analysis initial conditions. (Not implemented.)

`INSERT` Insert a node number. (Make a gap.)

`LIST` List the circuit on the console.

`LOG` Save a record of commands.

`MARK` Mark this time point, so transient analysis will restart here.

`MERGE` Get a circuit from disk. Add it the what is already in memory.

`MODIFY` Change a value, node, etc. For very simple changes.

`NODESET` Preset node voltages, to assist convergence. (Not implemented.)

`NOISE` SPICE command not implemented.

`OP` Performs a nonlinear DC analysis, for determining quiescent operating conditions. Sweeps temperature.

`OPTIONS` View and set system options. (Same as set.)

`PAUSE` Wait for key hit, while in batch mode.

`PLOT` Select points in circuit (and their range) to plot.

`PRINT` Select which points in the circuit to print as table.

`QUIT` Exits the program. (Same as exit.)

`SAVE` Save the circuit in a file.

`SENS` SPICE command not implemented.

`STATUS` Display resource usage, etc.

`SWEEP` Sweep a component. (Loop function.)

`TEMP` SPICE command not implemented.

`TF` SPICE command not implemented.

`TITLE` View and create the heading line for printouts and files.

`TRANSIENT` Performs a nonlinear transient (time domain) analysis. Sweeps time.

`UNFAULT` Undo faults.

`UNMARK` Undo mark. Release transient start point.

`WIDTH` Set output width.

2.2 ! command

2.2.1 Syntax

`!` *command*

2.2.2 Purpose

Run a program, or escape to a shell.

2.2.3 Comments

Any *command* typed here will be passed to the system for it to execute.

The bare command `!` will spawn an interactive shell. Exiting the shell will return.

2.2.4 Examples

`! ls *.ckt` Run the command `ls *.ckt` as if it were a shell command.

`!` No arguments mean to spawn an interactive shell.

2.3 < command

2.3.1 Syntax

`<` *filename*
`<<` *filename*

2.3.2 Purpose

Run a simulation in batch mode. Gets the commands and circuit from a disk file. `<<` clears the old circuit, first.

2.3.3 Comments

You can invoke the batch mode directly from the command that starts the program. The first command line argument is considered to be an argument for this command.

The file format is almost as you would type it on the keyboard. Commands must be prefixed with a dot, and circuit elements can be entered directly, as if in *build* mode. This is compatible with Spice.

The `log` command makes a file as you work the program, but the format is not correct for this command. To fix it, prefix commands with a dot, and remove the `build` commands.

Any line that starts with `*` a comment line.

Any line that starts with `.` (dot) is a command.

Any line that starts with a letter is a component to be added or changed.

A `<` command in the file transfers control to a new file. Files can be nested.

A bare `<` in the file (or the end of the file) gives it back to the console.

Unlike SPICE, commands are executed in order. This can result in some surprises when using some SPICE files. SPICE queues up commands, then executes them in a predetermined order.

2.3.4 Examples

`< thisone.ckt` Activates batch mode, from the file `thisone.ckt`, in the current directory.

`< runit.bat` Use the file `runit.bat`.

From the shell: on start up:

`acs afile` Start up the program. Start using the file `afile.ckt` in batch mode, as if you entered `< afile` as the first command.

`acs <afile` Start up the program. Start using the file `afile.ckt` with commands as if you typed them from the keyboard.

2.4 > command

2.4.1 Syntax

> *file*
>> *file*
>

2.4.2 Purpose

Saves a copy of all program output (except help) in a file.

2.4.3 Comments

> creates a new file for this output. If the file already exists, the old one is lost, and replaced by the new one.

>> appends to an existing file, if it exists, otherwise it creates one.

A bare > closes the file.

2.4.4 Examples

`> run1` Save everything in a file `run1` in the current directory. If `run1` already exists, the old one is gone.

`>> allof` Save everything in a file `allof`. If `allof` already exists, it is kept, and the new data is added to the end.

> Close the file. Stop saving.

2.5 AC command

2.5.1 Syntax

`AC` {*options ...*} *start stop stepsize* {*options ...*}

2.5.2 Purpose

Performs a small signal, steady state, AC analysis. Sweeps frequency.

2.5.3 Comments

The AC command does a linear analysis about an operating point. *It is absolutely necessary to do an* `OP` *analysis first on any nonlinear circuit. Not doing this is the equivalent of testing it with the power off.*

Three parameters are normally needed for an AC analysis: start frequency, stop frequency and step size, in this order. If all of these are omitted, the values from the most recent AC analysis are used.

If only one frequency is specified, a single point analysis will be done.

If only a new step size is specified, the old start and stop are kept and only the step size is changed. This is indicated by a keyword: `by`, `times`, `decade` or `octave`, or a symbol: `+` or `*`.

If the start frequency is zero, the program will still do an AC analysis. The actual frequency can be considered to be the limit as the frequency approaches zero. It is, therefore, still possible to have a non-zero phase angle, but delays are not shown because they may be infinite.

The nodes to look at must have been previously selected by the `print` or `plot` command. This is different fron Spice.

2.5.4 Options

`+` *stepsize* Linear sweep. Add *stepsize* to get the next step. Same as `By`.

`*` *multiplier* Log sweep. Multiply by *multiplier* to get the next step.

`>` *file* Send results of analysis to *file*.

`>>` *file* Append results to *file*.

`By` *stepsize* Linear sweep. Add *stepsize* to get the next step. Same as `+`.

`Decade` *steps* Log sweep. Use *steps* steps per decade.

`NOPlot` Suppress plotting.

`Octave` *steps* Log sweep. Use *steps* steps per octave.

`PLot` Graphic output, when plotting is normally off.

`Print` Send results to printer.

`Quiet` Suppress console output.

`TEmperature` *degrees* Temperature, degrees C.

`TImes` *multiplier* Log sweep. Multiply by *multiplier* to get the next step.

2.5.5 Examples

`ac 10m` A single point AC analysis at 10 mHz.

`ac 1000 3000 100` Sweep from 1000 Hz to 3000 Hz in 100 Hz steps.

`ac 1000 3000 Octave` Sweep from 1000 Hz to 3000 Hz in octave steps. Since the sweep cannot end at 3000 Hz, in this case, the last step will really be 4000 Hz.

`ac by 250` Keep the same limits as before, but use 250 Hz steps. In this case, it means to sweep from 1000 to 3000 Hz, because that it what it was the last time.

`ac 5000 1000 -250` You can sweep downward, if you want. Remember that the increment would be negative.

`ac 20 20k *2` Double the frequency to get the next step.

`ac 20k 20 *.5` You can do a log sweep downward, too. A multiplier of less than one moves it down.

`ac` Do the same AC sweep again.

`ac >afile` Save the results in the file `afile`. The file will look just like the screen. It will have all probe points. It will be a plot, if plotting is enabled. It will have the numbers in abbreviated notation. (10 nanovolts is `10.n`.)

2.6 `ALARM` command

2.6.1 Syntax

`ALArm`
`ALArm` *mode points ... ...*
`ALArm` *mode + points ... ...*
`ALArm` *mode - points ... ...*
`ALArm` *mode* CLEAR

2.6.2 Purpose

Select points in the circuit to check against user defined limits.

2.6.3 Comments

The '`alarm`' command selects points in the circuit to check against limits. There is no output unless the limits are exceeded. If the limits are exceeded a the value is printed.

There are separate lists of probe points for each type of analysis.

To list the points, use the bare command '`alarm`'.

Syntax for each point is *parameter(node)(limits)*, *parameter(componentlabel)(limits)*, or *parameter(index)(limits)*. Some require a dummy index.

For more information on the data available see the `print` command.

You can add to or delete from an existing list by prefixing with `+` or `-`. `alarm ac + v(3)` adds v(3) to the existing set of AC probes. `alarm ac - q(c5)` removes q(c5) from the list. You can use the wildcard characters `*` and `?` when deleting.

2.6.4 Examples

`alarm ac vm(12)(0,5) vm(13)(-5,5)` Check magnitude of the voltage at node 12 against a range of 0 to 5, and node 13 against a range of -5 to 5 for AC analysis. Print a warning when the limits are exceeded.

`alarm op id(m*)(-100n,100n)` Check current in all mosfets. In op analysis, print a warning for any that are outside the range of -100 to +100 nanoamps. The range goes both positive and negative so it is valid for both N and P channel fets.

`alarm tran v(r83)(0,5) p(r83)(0,1u)` Check the voltage and power of `R83` in the next transient analysis. The voltage range is 0 to 5. The power range is 0 to 1 microwatt. Print a warning when the range is exceeded.

`alarm` List all the probes for all modes.

`alarm dc` Display the DC alarm list.

`alarm ac CLear` Clear the AC list.

2.7 ALTER command

The Spice `Alter` command is not implemented. Similar functionality is available from the `sweep` command.

2.8 BUILD command

2.8.1 Syntax

`Build` {*line*}

2.8.2 Purpose

Builds a new circuit, or replaces lines in an existing one.

2.8.3 Comments

`Build` Lets you enter the circuit from the keyboard. The prompt changes to `>` to show that the program is in the build mode.

At this point, type in the circuit components in standard (Spice type) netlist format.

Component labels must be unique. If not, the old one is modified according to the new data, keeping old values where no new ones were specified.

Ordinarily, components are added to the end of the list. To insert at a particular place, specify the label to insert in front of. Example: `Build R77` will cause new items to be added before `R77`, instead of at the end.

In either case, components being changed or replaced do not change their location in the list.

If it is necessary to start over, `delete all` or `clear` will erase the entire circuit in memory.

To exit this mode, enter a blank line.

2.8.4 Examples

`build` Build a circuit. Add to the end of the list. This will add to the circuit without erasing anything. It will continue until you exit or memory fills up.

`b` This is the same as the previous example. Only the first letter of the 'Build' is necessary.

`build R33` Insert new items in front of R33.

2.9 CHDIR command

2.9.1 Syntax

`ChDir` {*path*}
`CD` {*path*}

2.9.2 Purpose

Changes or displays the current directory name.

2.9.3 Comments

Change the current directory to that specified by *path*. See your system manual for complete syntax.

If no argument is given the current directory is displayed.

2.9.4 Examples

`cd ../ckt` Change the current working directory to `../ckt`.

`cd` Show the current working directory name.

2.10 CLEAR command

2.10.1 Syntax

`CLEAR`

2.10.2 Purpose

Deletes the entire circuit, and blanks the title.

2.10.3 Comments

The entire word `clear` is required.

`Clear` is similar to, but a little more drastic than `delete all`.

After deleting anything, there is no way to get it back.

See also: `delete` command.

2.10.4 Examples

`clear` Delete the entire circuit.

2.11 `DC` command

2.11.1 Syntax

`DC` *start stop stepsize* {*options ...*}
`DC` *label start stop stepsize* {*options ...*}

2.11.2 Purpose

Performs a nonlinear DC steady state analysis, and sweeps the signal input, or a component value.

2.11.3 Status

Nesting of sweeps is not supported. (SPICE supports two levels of nesting.)

2.11.4 Comments

The nodes to look at must have been previously selected by the `print` or `plot` command.

If there are numeric arguments, without a part label, they represent a ramp from the `generator` function. They are the start value, stop value and step size, in order. They are saved between commands, so no arguments will repeat the previous sweep.

A single parameter represents a single input voltage. Two parameters instruct the computer to analyze for those two points only.

In some cases, you will get one more step outside the specified range of inputs due to internal rounding errors. The last input may be beyond the end point.

This command also sets up a movable operating point for subsequent `AC` analysis, which can be helpful in distortion analysis.

The program will sweep any simple component, including resistors, capacitors, and controlled sources. SPICE sweeps only fixed sources (types `V` and `I`).

2.11.5 Options

`*` *multiplier* Log sweep. Multiply the input by *multiplier* to get the next step. Do not pass zero volts!!

`>` *file* Send results of analysis to *file*.

`>>` *file* Append results to *file*.

`BY` *stepsize* Linear sweep. Add *stepsize* to get the next step.

`Continue` Use the last step of a `OP`, `DC` or `Transient` analysis as the first guess.

`Decade` *steps* Log sweep. Use *steps* steps per decade.

`LOop` Repeat the sweep, backwards.

`NOPlot` Suppress plotting.

`PLot` Graphic output, when plotting is normally off.

`Print` Send results to printer.

`Quiet` Suppress console output.

`REverse` Sweep in the opposite direction.

`TEmperature` *degrees* Temperature, degrees C.

`Times` *multiplier* Log sweep. Multiply the input by *multiplier* to get the next step. Do not pass zero volts!!

`TRace` *n* Show extended information during solution. Must be followed by one of the following:

- `Off` No extended trace information (default, override .opt)
- `Warnings` Show extended warnings
- `Iterations` Show every iteration.
- `Verbose` Show extended diagnostics.

2.11.6 Examples

`dc 1` Do a single point DC signal simulation, with '1 volt' input.

`dc -10 15 1` Sweep the circuit input from -10 to +15 in steps of 1. (usually volts.) Do a DC transfer simulation at each step.

`dc` With no parameters, it uses the same ones as the last time. In this case, from -10 to 15 in 1 volt steps.

`dc 20 0 -2` You can sweep downward, by asking for a negative increment. Sometimes, this will result in better convergence, or even different results! (For example, in the case of a bi-stable circuit.)

`dc` Since the last time used the `input` option, go back one more to find what the sweep parameters were. In this case, downward from 20 to 0 in steps of 2. (Because we did it 2 commands ago.)

`dc -2 2 .1 loop` After the sweep, do it again in the opposite direction. In this case, the sweep is -2 to +2 in steps of .1. After it gets to +2, it will go back, and sweep from +2 to -2 in steps of -.1. The plot will be superimposed on the up sweep. This way, you can see hysteresis in the circuit.

`dc temperature 75` Simulate at 75 degrees, this time. Since we didn't specify new sweep parameters, do the same as last time. (Without the loop.)

2.12 DELETE command

2.12.1 Syntax

`DELete` *label ...*
`DELete ALL`

2.12.2 Purpose

Remove a line, or a group of lines, from the circuit description.

2.12.3 Comments

To delete a part, by label, enter the label. (Example 'DEL R15'.) Wildcards '`*`' and '`?`' are allowed, in which case, all that match are deleted.

To delete the entire circuit, the entire word `ALL` must be entered. (Example 'DEL ALL'.)

After deleting anything, there is usually no way to get it back, but if a fault had been applied (see `fault` command) `restore` may have surprising results.

2.12.4 Examples

`delete all` Delete the entire circuit, but save the title.

`del R12` Delete `R12`.

`del R12 C3` Delete `R12` and `C3`.

`del R*` Delete all resistors. (Also, any models and subcircuits starting with `R`.)

2.13 DISTO command

The Spice `disto` command is not implemented. Similar functionality is not available.

2.14 EDIT command

2.14.1 Syntax

`Edit`
`Edit` *file*

2.14.2 Purpose

Use your editor to change the circuit.

2.14.3 Comments

The `edit` command runs your editor on a copy of the circuit in memory, then reloads it.

`Edit` *file* runs your editor on the specified *file*.

If you are only changing a component value, the `modify` command may be easier to use.

The program uses the `EDITOR` environment variable to find the editor to use. The command fails if there is no `EDITOR` defined.

2.14.4 Examples

`edit` Brings up your editor on the circuit.

`edit .acsrc` Edits the file `.acsrc` in your current directory.

2.15 `END` command

When run in batch mode from the shell, the `END` command cleans up and exits the program.

In script mode (< command) it ends the script and returns to the program prompt.

In interactive mode it exits the program.

2.16 `EXIT` command

2.16.1 Syntax

`EXIt`

2.16.2 Purpose

Terminates the program.

2.16.3 Comments

'`Quit`' also works.

Be sure you have saved everything you want to!

2.17 `FANOUT` command

2.17.1 Syntax

`FANout` {*nodes*}

2.17.2 Purpose

Lists connections to each node.

2.17.3 Comments

`Fanout` lists the line number and label of each part connected to each node. If both ends of a part are connected the same place, it is listed twice.

For a partial list, just specify the numbers. A number alone (`17`) says this branch alone. A trailing dash (`23-`) says from here to the end. A leading dash (`-33`) says from the start to here. Two numbers (`9 13`) specify a range.

2.17.4 Examples

`fanout` Lists all the nodes in the circuit, with their connections.

`fanout 99` List parts connecting to node 99.

`fanout 0` List the connections to node 0. (There must be at least one, unless you are editing a model.)

`fanout 78-` List connections to nodes 78 and up.

`fanout 124 127` List connections to nodes 124, 125, 126, 127.

2.18 `FAULT` command

2.18.1 Syntax

`FAult` *partlabel=value ...*

2.18.2 Purpose

Temporarily change a component value.

2.18.3 Comments

This command quickly changes the value of a component, usually with the intention that you will not want to save it.

If you apply this command to a nonlinear or otherwise strange part, it becomes ordinary and linear until the fault is removed.

It is an error to `fault` a model call.

If several components have the same label, the fault value applies to all of them. (They will all have the same value.)

The `unfault` command restores the old values.

2.18.4 Example

`fault R66=1k` R66 now has a value of 1k, regardless of what it was before.

`fault C12=220p L1=1u` C12 is 220 pf and L1 is 1 uH, for now.

`unfault` Clears all faults. It is back to what it was before.

2.19 FOURIER command

2.19.1 Syntax

`Fourier` *start stop stepsize* {*options ...*}

2.19.2 Purpose

Performs a nonlinear time domain (transient) analysis, but displays the results in the frequency domain.

Start, *stop*, and *stepsize* are frequencies.

2.19.3 Comments

This command is slightly different and more flexible than the SPICE counterpart. SPICE always gives you the fundamental and 9 harmonics. ACS will do the same if you only specify one frequency. SPICE has the probes on the same line. ACS requires you to specify the probes with the `print` command.

SPICE uses the last piece of a transient that was already done. ACS does its own transient analysis, continuing from where the most recent one left off, and choosing the step size to match the Fourier Transform to be done. Because of this the ACS Fourier analysis is much more accurate than SPICE.

The nodes to look at must have been previously selected by the `print` or `plot` command.

Three parameters are normally needed for a Fourier analysis: start frequency, stop frequency and step size, in this order.

If the start frequency is omitted it is assumed to be 0. The two remaining parameters are stop and step, such that stop > step.

If only one frequency is specified, it is assumed to be step size, which is equivalent to the fundamental frequency. The start frequency is zero and the stop frequency is set according the `harmonics` option (from the `options` command. The default is 9 harmonics.

If two frequencies are specified, they are stop and step. The order doesn't matter since stop is always larger than step.

Actually, this command does a nonlinear time domain analysis, then performs a Fourier transform on the data to get the frequency data. The transient analysis parameters (start, stop, step) are determined by the program as necessary to produce the desired spectral results. The internal time steps are selected to match the Fourier points, so there is no interpolation done.

The underlying transient analysis begins where the previous one left off. If you specify the "cold" option, it begins at time = 0. Often repeating a run will improve the accuracy by giving more time for initial transients to settle out.

See also: `Transient` command.

2.19.4 Options

`>` *file* Send results of analysis to *file*.

`>>` *file* Append results to *file*.

`Cold` Zero initial conditions. Cold start from power-up.

`Quiet` Suppress console output.

`SKip` *count* Force at least *count* internal transient time steps for each one used.

`STiff` Use a different integration method, that will suppress overshoot when the step size is too small.

`TEmperature` *degrees* Temperature, degrees C.

`TRACe` *n* Show extended information during solution. Must be followed by one of the following:

- `Off` No extended trace information (default, override .opt)
- `Warnings` Show extended warnings
- `Alltime` Show all accepted internal time steps.
- `Rejected` Show all internal time steps including rejected steps.
- `Iterations` Show every iteration.
- `Verbose` Show extended diagnostics.

2.19.5 Examples

`fourier 1Meg` Analyze the spectrum assuming a fundamental frequency of 1 mHz. Use the `harmonics` option to determine how many harmonics (usually 9) to display.

`fourier 40 20k 20` Analyze the spectrum from 40 Hz to 20 kHz in 20 Hz steps. This will result in a transient analysis with 25 micro-second steps. (1 / 40k). It will run for .05 second. (1 / 20).

`fourier 0 20k 20` Similar to the previous example, but show the DC and 20 Hz terms, also.

`fourier` No parameters mean use the same ones as the last time. In this case: from 0 to 20 kHz, in 20 Hz steps.

`fourier Skip 10` Do 10 transient steps internally for every step that is used. In this case it means to internally step at 2.5 micro-second, or 10 steps for every one actually used.

`fourier Cold` Restart at time = 0. This will show the spectrum of the power-on transient.

2.20 `GENERATOR` command

2.20.1 Syntax

`Generator` {*option-name=value ...*}

2.20.2 Purpose

Sets up an input waveform for `transient` and `Fourier` analysis. Emulates a laboratory type function generator.

2.20.3 Comments

This command sets up a singal source that is conceptually separate from the circuit. To use it, make the value of a component "generator(1)", or substitute a scale factor for the parameter.

The SPICE style input functions also work, but are considered to be part of the circuit, instead of part of the test equipment.

The parameters available are designed to emulate the controls on a function generator. There are actually two generators here: sine wave and pulse. If both are on (by setting non-zero parameters) the sine wave is modulated by the pulse, but either can be used alone.

Unless you change it, it is a unit-step function at time 0. The purpose of the command is to change it.

This command does not affect `AC` or `DC` analysis in any way. It is only for `transient` and `Fourier` analysis. In `AC` analysis, the input signal is always a sine wave at the analysis frequency.

Typical usage is the name of the control followed by its value, or just plain `Generator` to display the present values.

The actual time when switching takes place is ambiguous by one time step. If precise time switching is necessary, use the `Skip` option on the transient analysis command, to force more resolution. This ambiguity can usually be avoided by specifying finite rise and fall times.

2.20.4 Parameters

`Frequency` The frequency of the sine wave generator for a transient analysis. The sine wave is modulated by the pulse generator. A frequency of zero puts the pulse generator on line directly.

`Amplitude` The overall amplitude of the pulse and sine wave. A scale factor. It applies to everything except the *offset* and *init* values.

`Phase` The phase of the sine wave, at the instant it is first turned on.

`MAx` The amplitude of the pulse, when it is 'on'. (During the *width* time) If the sine wave is on (frequency not zero) this is the amplitude of the sine wave during the first part of the period. The *max* is scaled by *ampl*.

`MIn` The amplitude of the pulse, when it is 'off'. (After it falls, but before the next period begins.) Although we have called these *min* and *max*, there is no requirement that *max* be larger than *min*. If the sine wave is on, this is its amplitude during the second part of the period. The *min* is scaled by *ampl*.

`Offset` The DC offset applied to the entire signal, at all times after the initial delay. The *offset* is **not** scaled by *ampl*.

`Init` The initial value of the pulse generator output. It will have this value starting at time 0, until *Delay* time has elapsed. It will never return to this value, unless you restart at time 0.

`Rise` The rise time, or the time it takes to go from *MIn* to *MAx*, or for the first rise, *Init* to *MAx*. The rise is linear.

`Fall` The fall time. (The time required to go from *MAx* back to *MIn*.)

`Delay` The waiting time before the first rise.

`Width` The length of time the output of the generator has the value *Max*. A width of zero means that the output remains high for the remainder of the period. If you really want a width of zero, use a very small number, less than the step size.

`Period` The time for repetition of the pulse. It must be greater than the sum of rise + fall + width. A period of zero means that the signal is not periodic and so will not repeat.

2.20.5 Examples

The generator command ...

`gen` Display the present settings.

`gen Freq=1k` Sets the sine wave to 1 kHz. All other parameters are as they were before.

`gen Freq=0` Turns off the sine wave, leaving only the pulse.

`gen Ampl=0` Sets the amplitude to zero, which means the circuit has no input, except for possibly a DC offset.

`gen Period=.001 Freq=1m` Sets the period back to 1 millisecond. Applies 1 mHz modulation to the pulse, resulting in a pulsed sine wave. In this case, a 100 microsecond 10 volt burst, repeating every millisecond. Between bursts, you will get 2.5 volts, with reversed phase. The old values, in this case from 2 lines back (above) are kept. (`Ampl 5 Rise 10u Fall 10u` ...)

`gen Freq=60 Phase=90 Delay=.1` The sine wave frequency is 60 Hertz. Its phase is 90 degrees when it turns on, at time .1 seconds. It turns on sharply at the peak.

A component using it ...

`V12 1 0 generator(1)` Use the generator as the circuit input through this voltage source. The DC and AC values are 0.

`V12 1 0 tran generator(1) ac 10 dc 5` Same as before, except that the AC value is 10 and DC value is 5.

`Rinput 1 0 tran generator(1)` Unlike SPICE, the functions can be used on other components. The resistance varies in time according to the "generator".

2.21 GET command

2.21.1 Syntax

`GET` *filename*

2.21.2 Purpose

Gets an existing circuit file, after clearing memory.

2.21.3 Comments

The first comment line of the file being read is taken as the 'title'. See the `title` command.

Comments in the circuit file are stored, unless they start with `*+` in which case they are thrown away.

'Dot cards' are set up, but not executed. This means that variables and options are changed, but simulation commands are not actually done. As an example, the `options` command is actually performed, since it only sets up variables. The `ac` card is not performed, but its parameters are stored, so that a plain `ac` command will perform the analysis specified in the file.

Any circuit already in memory will be erased before loading the new circuit.

2.21.4 Examples

`get amp.ckt` Get the circuit file `amp.ckt` from the current directory.

`get /usr/foo/ckt/amp.ckt` Get the file `amp.ckt` from the `/usr/foo/ckt` directory.

`get npn.mod` Get the file `npn.mod`.

2.22 IC command

The Spice `IC` command is not implemented. Similar functionality is not available.

2.23 INSERT command

2.23.1 Syntax

`INsert` *node*
`INsert` *node, count*

2.23.2 Purpose

Open up node numbers inside a circuit.

2.23.3 Comments

To open up an internal node, enter `insert` followed by the number and how many. All node numbers higher than the first number will be raised by the second. The second (how many) is optional. If omitted, 1 will be assumed.

2.23.4 Examples

`insert 8 3` Insert 3 nodes before node 8. Adds 3 nodes (8,9,10) with no connections. Old node numbers 8 and higher have 3 added to them to make room. Old node 8 is now 11, 9 is now 12, 10 is now 13, 11 is 14, etc.

`insert 6` Insert one node at 6. Old nodes 6 and higher are incremented by 1. Old node 6 is now 7, 7 is 8, etc.

2.24 LIST command

2.24.1 Syntax

`List` {*label ...*}
`List` {*label - label*}

2.24.2 Purpose

Lists the circuit in memory.

2.24.3 Comments

Plain `List` will list the whole circuit on the console.

`List` with a component label asks for that one only. Wildcards are supported: `?` matches any character, once. `*` matches zero or more of any character.

For several components, list them.

For a range, specify two labels separated by a dash.

2.24.4 Examples

`list` List the entire circuit to the console.

`list R11` Show the component `R11`.

`list D12 - C5` List the part of the netlist from `M12` to `C5`, inclusive. `D12` must be before `C5` in the list.

`list D* C*` List all diodes and capacitors.

2.25 LOG command

2.25.1 Syntax

`LOg` *file*
`LOg >>` *file*
`LOg`

2.25.2 Purpose

Saves a copy of your keyboard entries in a file.

2.25.3 Comments

The '`>>`' option appends to an existing file, if it exists, otherwise it creates one.

Files can be nested. If you open one while another is already open, both will contain all the information.

A bare LOg closes the file. Because of this, the last line of this file is always LOg. Ordinarily, this will not be of any consequence, but if a log file is open when you use this file as command input, this will close it. If more than one LOg file is open, they will be closed in the reverse of the order in which they were opened, maintaining nesting.

See also: '>' and '<' commands.

2.25.4 Bugs

The file is an exact copy of what you type, so it is suitable for acs <file from the shell. It is NOT suitable for the < command in acs or the Spice-like mode acs file without <.

2.25.5 Examples

log today Save the commands in a file today in the current directory. If today already exists, the old one is gone.

log >> doit Save the commands in a file doit. If doit already exists, it is kept, and the new data is added to the end.

log runit.bat Use the file runit.bat.

log Close the file. Stop saving.

2.26 MARK command

2.26.1 Syntax

MArk

2.26.2 Purpose

Remember circuit voltages and currents.

2.26.3 Comments

After the mark command, the transient and fourier analysis will continue from the values that were kept by the mark command, instead of progressing every time.

This allows reruns from the same starting point, which may be at any time, not necessarily 0.

2.26.4 Examples

transient 0 1 .01 A transient analysis starting at zero, running until 1 second, with step size .01 seconds. After this run, the clock is at 1 second.

mark Remember the time, voltages, currents, etc.

transient Another transient analysis. It continues from 1 second, to 2 seconds. (It spans 1 second, as before.) This command was not affected by the mark command.

transient This will do exactly the same as the last one. From 1 second to 2 seconds. If it were not for mark, it would have started from 2 seconds.

transient 1.5 .001 Try again with smaller steps. Again, it starts at 1 second.

unmark Release the effect of mark.

transient Exactly the same as the last time, as if we didn't unmark. (1 to 1.5 seconds.)

transient This one continues from where the last one left off: at 1.5 seconds. From now on, time will move forward.

2.27 MERGE command

2.27.1 Syntax

MErge *filename*

2.27.2 Purpose

Gets an existing circuit file, without clearing memory.

2.27.3 Comments

The first comment line of the file being read is the new title, and replaces the existing title.

Comments in the circuit file are stored, unless they start with *+ in which case they are thrown away.

'Dot cards' are set up, but not executed. This means that variables and options are changed, but simulation commands are not actually done. As an example, the options command is actually performed, since it only sets up variables. The ac command is not performed, but its parameters are stored,

so that a plain `ac` command will perform the analysis specified in the file.

Any circuit already in memory is kept. New elements with duplicate labels replace the old ones. New elements that are not duplicates are added to the end of the list, as if the files were appended.

2.27.4 Examples

`merge amp.ckt` Get the circuit file `amp.ckt` from the current directory. Use it to change the circuit in memory.

`merge npn.mod` Include the file `npn.mod`.

2.28 `MODIFY` command

2.28.1 Syntax

`MOdify` *partlabel=value ...*

2.28.2 Purpose

Quickly change a component value.

2.28.3 Comments

This command quickly changes the value of a component. It is restricted to simply changing the value.

If several components have the same label or if wildcard characters are used, all are changed.

2.28.4 Example

`modify R66=1k` R66 now has a value of 1k, regardless of what it was before.

`modify C12=220p L1=1u` C12 is 220 pf and L1 is 1 uH.

`mod R*=22k` All resistors are now 22k.

2.29 `NODESET` command

The Spice `NODESET` command is not implemented. Similar functionality is not available.

2.30 `NOISE` command

The Spice `NOIse` command is not implemented. Similar functionality is not available.

2.31 `OP` command

2.31.1 Syntax

`OP` *start stop stepsize* {*options ...*}

2.31.2 Purpose

Performs a nonlinear DC steady state analysis, with no input. If a temperature range is given, it sweeps the temperature.

2.31.3 Comments

There are substantial extensions beyond the capabilities of the SPICE `op` command.

If there are numeric arguments, they represent a temperature sweep. They are the start and stop temperatures in degrees Celsius, and the step size, in order. They are saved between commands, so no arguments will repeat the previous sweep.

This command will use the `op` probe set, instead of automatically printing all nodes and source currents, so you must do "`print op` ...." before running op. We did it this way because we believe that printing everything all the time is usually unnecessary clutter. All of the information available from SPICE and more is available here. See the `print` command and the device descriptions for more details.

A single parameter represents a single temperature. Two parameters instruct the computer to analyze for those two points only.

This command also sets up the quiescent point for subsequent `AC` analysis. It is necessary to do this for nonlinear circuits. The last step in the sweep determines the quiescent point for the AC analysis.

2.31.4 Options

`*` *multiplier* Log sweep. Multiply the *absolute* temperature by *multiplier* to get the next step. The fact that it is offset to absolute zero may make the step sizes look strange.

> *file* Send results of analysis to *file*.

>> *file* Append results to *file*.

BY *stepsize* Linear sweep. Add *stepsize* to get the next step.

Continue Use the last step of a OP, DC or Transient analysis as the first guess.

Input *volts* Apply *volts* input to the circuit, instead of zero.

LOop Repeat the sweep, backwards.

PLot Graphic output, when plotting is normally off.

Print Send results to printer.

Quiet Suppress console output.

REverse Sweep in the opposite direction.

TAble Tabular output. Override default plot.

TEmperature *degrees* Temperature, degrees C. Override the sweep.

TImes *multiplier* Log sweep. Multiply the **absolute** temperature by *multiplier* to get the next step.

TRace *n* Show extended information during solution. Must be followed by one of the following:

Off No extended trace information (default, override .opt)

Warnings Show extended warnings

Iterations Show every iteration.

Verbose Show extended diagnostics.

2.31.5 Examples

op 27 Do a DC operating point simulation at temperature 27 degrees Celsius.

op -50 200 25 Sweep the temperature from -50 to 200 in 25 degree steps. Do a DC operating point simulation at each step.

op With no parameters, it uses the same ones as the last time. In this case, from -50 to 200 in 25 degree steps.

op 200 -50 -25 You can sweep downward, by asking for a negative increment.

op Input 2.3 Apply an input to the circuit of 2.3 volts. This overrides the default of no input.

op TEmperature 75 Simulate at 75 degrees, this time. This isn't remembered for next time.

op Since the last time used the TEmperature option, go back one more to find what the sweep parameters were. In this case, downward from 200 to -50 in 25 degree steps. (Because we did it 3 commands ago.)

2.32 OPTIONS command

2.32.1 Syntax

OPTions
OPTions *option-name value* ...

2.32.2 Purpose

Sets options, iteration parameters, global data.

2.32.3 Comments

Typical usage is the name of the item to set followed by the value.

The bare command 'OPTions' displays the values.

These options control the simulation by specifying how to handle marginal circumstances, how long to wait for convergence, etc.

Most of the SPICE options are supported, more have been added.

2.32.4 Parameters

ACCT Turns on accounting. When enabled, print the CPU time used after each command, and a summary on exit in batch more. This does not affect accounting done by the status command.

NOACCT Turns off accounting. (Not in SPICE.)

LIST Turns on echo of files read by get and merge commands, and in batch mode. (SPICE option accepted but not implemented.)

NOLIST Turns off list option. (Not in SPICE.)

MOD Enable printout of model parameters. (Accepted, but not implemented, to complement NOMOD.)

NOMOD Suppress printout of model parameters. (SPICE option accepted but not implemented.)

PAGE Enable page ejects at the beginning of simulation runs. (Accepted, but not implemented, to complement NOPAGE.)

NOPAGE Turn off page ejects. (SPICE option accepted but not implemented.)

NODE Enable printing of the node table. (SPICE option accepted but not implemented.)

NONODE Disable printing of the node table. (Accepted, but not implemented, to complement NODE.)

OPTS Enable printing of option values on every options command.

NOOPTS Disable automatic printing of option values. Option values are only printed on a null options command.

GMIN = x Minimum conductance allowed by the program. (Default = 1e-12 or 1 picomho.) Every node must have a net minimum conductance of GMIN to ground. If effective open circuits are found during the solution process (leading to a singular matrix) a conductance of GMIN is forced to ground, after printing an "open circuit" error message.

RELTOL = x Relative error tolerance allowed. (Default =.001 or .1%.) If the ratio of successive values in iteration are within RELTOL of one, this value is considered to have converged.

ABSTOL = x Absolute error tolerance allowed. (Default = 1e-12) If successive values in iteration are within ABSTOL of each other, this value is considered to have converged.

VNTOL = x Absolute voltage error required to force model re-evaluation. (Default = 1e-12 or 1 microvolt.) If the voltage at the terminals of a model is within VNTOL of the previous iteration, the model is not re-evaluated. The old values are used directly.

TRTOL = x Transient error "tolerance". (Default = 7.) This parameter is an estimate of the factor by which the program overestimates the actual truncation error.

CHGTOL = x Charge tolerance. (Default = 1e-14) It is used in step size control in transient analysis.

PIVTOL = x Pivot tolerance. (Default = 1e-13) SPICE option accepted but not implemented.

PIVREL = x Pivot ratio. (Default = 1e-3) SPICE option accepted but not implemented.

NUMDGT = x Number of significant digits to print. (Default = 4.) SPICE option accepted but not implemented.

TNOM = x Nominal temperature. (Default = 27° C.) All components have their nominal value at this temperature.

ITL1 = x DC iteration limit. (Default = 100.) Sets the maximum number of iterations in a DC, OP, or initial transient analysis allowed before stopping and reporting that it did not converge.

ITL2 = x DC transfer curve iteration limit. (Default = 50.) SPICE option accepted but not implemented. Use ITL1 instead.

ITL3 = x Lower transient iteration limit. (Default = 4.) If the number of iterations is more than ITL3 the step size will not increase beyond its present size. Otherwise, it can grow by trstepgrow.

ITL4 = x Upper transient iteration limit. (Default = 10.) Sets the maximum number of iterations on a step in transient analysis. If the circuit fails to converge in this many iterations the step size is reduced (by option trstepshrink), time is backed up, and the calculation is repeated.

ITL5 = x Transient analysis total iteration limit. (Default = 5000.) SPICE option accepted but not implemented. Actual behavior is the same as ITL5 = 0, in SPICE, which omits this test.

ITL6 = x Source stepping iteration limit. (Default = 0.) SPICE option accepted but not implemented. Source stepping is not available.

ITL7 = x Worst case analysis iteration limit. (Default = 1.) Sets the maximum number of iterations for the individual element trials in a DC or bias worst case analysis. If more iterations than this are necessary, the program silently goes on to the next step, as if nothing was wrong, which is usually the case.

ITL8 = x Convergence diagnostic iteration threshold. (Default = 100.) If the iteration count on a step exceeds ITL8 diagnostic messages are printed in an attempt to aid the user in solving the convergence problem.

CPTIME = x Total CPU job time limit. (Default = 30000.) SPICE option accepted but not implemented. There is no limit imposed.

LIMTIM = x CPU time reserved for plotting. (Default = 2.) SPICE option accepted but not implemented.

LIMPTS = x Max number of points printed. (Default = 201.) SPICE option accepted but not implemented.

LVLCOD = x Matrix solution and allocation method. (Default = 2, generate machine language.) SPICE option not implemented.

LVLTIM = x Time step control method. (Default = 2, truncation error.) SPICE option not implemented.

METHOD = x Integration method. (Default = TRAPezoidal.) Possible values are:

EULER backward Euler, unless forced to other

EULERONLY backward Euler only

TRAP usually trap, but Euler where better

TRAPONLY always trapezoid

DEFL = x MOSFET default channel length in meters. (Default = 100u.)

DEFW = x MOSFET default channel width in meters. (Default = 100u.)

DEFAD = x MOSFET default drain diffusion area in square meters. (Default = 0.)

DEFAS = x MOSFET default source diffusion area in square meters. (Default = 0.)

SEED = x Seed used by the random number generator. (Default = 1.) (ECA-2 equivalent = Random.) (Not available in SPICE.) The same random numbers will be used every time, determined by this seed number. Setting this to zero is a special case, causing each run to start from a random point.

WCZERO = x Worst case zero window. (Default = 1e-9) (Not available in SPICE.) Sets a window for the difference in a DC or bias worst case analysis. Differences less than this are assumed to be zero, for purposes of setting direction flags. This prevents cluttering up the screen with very small numbers that are essentially zero.

DAMPMAX = x Normal Newton damping factor. (Default = 1.) Sets the damping factor for iteration by damped Newton's method, used when all is well. It must be between 0 and 1, as close to 1 as possible and still achieve convergence. The useful range is from .9 to 1. Setting DAMPMAX too low will probably cause convergence to a nonsense result.

DAMPMIN = x Newton damping factor in problem cases. (Default = .5) Sets the damping factor for iteration by damped Newton's method, used when there are problems. It must be between 0 and 1, and is usually set somewhat less than DAMPMAX. The useful range is from .5 to .9. Setting it lower than .5 may cause convergence to a nonsense result. Aside from that, a lower value (but less than DAMPMAX) tends to improve robustness at the expense of convergence speed.

DAMPSTrategy = x Damping strategy. (Default = 0) The actual damping factor to use is determined by heuristics. Normally the damping factor is DAMPMAX. It is reduced to DAMPMIN when certain conditions occur, then it drifts back up on subsequent iterations. This parameter turns the various heuristics on or off. The number to use is the sum of the following flags.

1 the second iteration on any voltage or time step. (usually helps robustness, but always increases iteration count.)

2 if the voltage at any nonlinear node exceeds the range determined by `VMIN`, `VMAX`, and `LIMIT`. (usually not desirable.)

4 if any device limiting algorithm is activated. (usually not desirable.)

10 when any device crosses a region boundary. (usually desirable and has little cost.)

20 when a FET or BJT is reversed. (usually helps robustness. sometimes increases iteration count.)

`FLOOR` = x Effective zero value. (Default = 1e-20) Results values less than FLOOR are shown as zero.

`TEMPAMB` = x Simulation temperature. (Default = 27° C.) Sets the ambient temperature, in degrees Celsius. This is the temperature at which the simulation takes place, unless changed by some other command.

`Short` = x Resistance of voltage source or short. (Default = 1e-7 or 10 $\mu\Omega$.) Sets the default resistance of voltage sources. In some cases, inductors are replaced by resistors, if so, this is the value. It is also the resistance used to replace short circuits anywhere they are not allowed and the program finds one.

`TRansits` = x Mixed mode transition count. (Default = 2) Sets the number of "good" transitions for a supposedly digital signal to be accepted as digital.

`IN` = x Input width. (Default = 80.) Sets the last column read from each line of input. Columns past this are ignored. This option is present only for SPICE compatibility, through the `width` command, which is an alias for `options`.

`OUT` = x Output width. (Default = 80.) Sets the output print width, for tables and character graphics.

`XDivisions` = x X axis divisions. (Default = 4) Sets the number of divisions on the X axis for plotting.

`YDivisions` = x Y axis divisions. (Default = 4) Sets the number of divisions on the Y axis for plotting.

`ORder` = x Equation ordering. (Default = auto.) Determines how external node numbers are mapped to internal numbers. The values are `FORward`, `REVerse`, and `AUTo`.

`MODe` = x Simulation mode selection. (Default = mixed.) Values are `ANAlog`, `DIGital`, and `MIXed`. In analog mode, logic elements (type U) are replaced by their subcircuits as if they were type X. In digital mode, logic elements are simulated as digital regardless of whether the signals are proper or not, as in traditional mixed-mode simulation. In mixed mode, logic elements may be simulated as analog or digital depending on the signals present.

`BYPass` Bypass model evaluation if appropriate. If the last two iterations indicate that an element is converged or dormant, do not evaluate it but use its old values directly. (Default)

`VBYpass` Check only voltage to bypass model evaluation. This produces a faster but possibly less accurate simulation.

`NOBYpass` Do not bypass model evaluation.

`LUBypass` Bypass parts of LU decomposition if appropriate. If only a few elements of the matrix were changed solve only those parts of the LU matrix that depend on them. (Default)

`NOLUbypass` Do not bypass parts of LU decomposition. Solve the entire LU matrix whenever a matrix solution is called for regardless of whether it is actually needed.

`INCmode` Incrementally update the matrix. Instead of rebuilding the matrix on every iteration, keep as much of the old matrix as possible and make incremental changes. (Default)

`NOIncmode` Do not incrementally update the matrix. This eliminates a possible cause of roundoff error at the expense of a slower simulation.

`TRACELoad` Use a queue to only load changed elements to the matrix. This results in faster loading and has no known drawbacks. (Default)

`NOTRACELoad` Do not use a queue to only load changed elements to the matrix. Instead, load all elements, even if they are unchanged or zero. This is always slower, and is forced if "noincmode".

`LIMIT` = x Internal differential branch voltage limit. (Default = 1e10, essentially disabled.) All circuit branch voltages may be limited to $\pm x$ to aid in convergence. This is intended as a convergence aid only. It may or may not help.

`VMIN` = x Negative node voltage limit. (Default = -30) All node voltages may be limited to $-x$ to aid in convergence and prevent numeric overflow. This is intended as a convergence aid only. It may or may not help.

`VMAX` = x Positive node voltage limit. (Default = 30) All node voltages may be limited to $+x$ to aid in convergence and prevent numeric overflow. This is intended as a convergence aid only. It may or may not help.

`DTMIn` = x Minimum time step. (Default = 1e-12.) The smallest internal time step in transient analysis. The `transient` command `dtmin` option and the `dtratio` option override it if it is bigger.

`DTRatio` = x The ratio between minimum and maximum time step. (Default = 1e9).

`RSTray` Include series resistance in device models. This creates internal nodes and results in a significant speed and memory penalty. It also makes convergence characteristics worse.

`NORSTray` Do not include series resistance in device models. This results in faster simulations and better numerical accuracy at the expense of model accuracy. Differences between `rstray` and `norstray` have been observed to be insignificant most of the time. Some popular commercial versions of SPICE do not implement series resistance at all, so `norstray` may be more consistent with other simulators.(Default)

`CSTray` Include capacitance in device models. This may create internal nodes and result in a significant speed and memory penalty. It also may make convergence characteristics worse. (Default)

`NOCSTray` Do not include capacitance in device models. This results in faster simulations and better numerical accuracy at the expense of model accuracy. Differences between `cstray` and `nocstray` are usually significant, since often the strays are the dominant reactive elements.

`Harmonics` = x Harmonics in Fourier analysis. (Default = 9) The number of harmonics to display in a Fourier analysis, unless specified otherwise.

`TRSTEPGrow` = x The maximum internal step size growth in transient analysis. (Default = 2.)

`TRSTEPShrink` = x The amount to decrease the transient step size by when convergence fails. (Default = 8.)

`TRReject` = x Transient error rejection threshold. (Default = .5) Controls how bad the truncation error must be to reject a time step. A value of .5 means that if the step reqested is smaller than .5 times the step size used, the current step will be rejected. If the new step is .8 times the old step size it will be adjusted but the step just calculated will not be rejected.

2.32.5 Examples

`options` Display the present settings.

`options itl1=50` Allows 50 iterations in a `dc` or `op` analysis.

2.33 PAUSE command

2.33.1 Syntax

`PAuse` *comment*

2.33.2 Purpose

Suspend batch mode. Wait for the user to hit a key.

2.33.3 Status

This command does not work on all systems, due to buffering of console i/o.

2.33.4 Comments

Prints `Continue?` and waits for a key hit. Type '`n`', '`N`', escape or control-c to terminate the batch mode. Type anything else to continue.

Any *comment* is ignored.

2.33.5 Examples

```
pause Try more gain
```

`pause` These both work the same. Ask to continue, wait for a key hit, then go on.

2.34 `PLOT` command

2.34.1 Syntax

`PLot`
`PLot` *mode points ... ...*
`PLot` *mode + points ... ...*
`PLot` *mode - points ... ...*
`PLot` *mode* CLEAR

2.34.2 Purpose

Select points in the circuit for graphic output. Select graphic output.

2.34.3 Status

The plotting leaves something to be desired. Only two signals can be plotted at a time. The output file is corrupt when plotting is on.

2.34.4 Comments

The '`plot`' command selects where to look at the circuit, or where to hook the oscilloscope probe.

There are separate lists of probe points for each type of analysis.

To list the probe points, use the bare command '`plot`'.

Syntax for each point is *parameter(node)(limits)*, *parameter(componentlabel)(limits)*, or *parameter(index)(limits)*. Some require a dummy index.

For more information on the data available see the `print` command.

You must set the scaling. If you do not, the default range is fixed at -5 to 5. ACS cannot auto-scale because it generates the plot during simulation, so the necessary information is not available yet. Spice can auto-scale only because it waits for the simulation to complete before producing any output.

`Plot` uses the same variables as `print`. See the print command for a list of what is available.

The options `plot` and `noplot` on any analysis command turn plotting on and off a single run. The `plot` command turns plotting on and tabular output off. The `print` command turns plotting off and tabular output on.

You can add to or delete from an existing list by prefixing with `+` or `-`. `plot ac + v(3)` adds v(3) to the existing set of AC probes. `plot ac - q(c5)` removes q(c5) from the list. You can use the wildcard characters `*` and `?` when deleting.

Plotting is limited to 2 items.

2.34.5 Examples

`plot ac vm(12)(0,5) vm(13)(-5,5)` The magnitude of the voltage at node 12 with a range of 0 to 5, and node 13 with a range of -5 to 5 for AC analysis.

`plot dc v(r26)` The voltage across `R26` for DC analysis. Since there is no range, default values will be used.

`plot tran v(r83)(0,5) p(r83)(0,1u)` Plot the voltage and power of `R83` in the next transient analysis. The voltage scale is 0 to 5. The power scale is 0 to 1 microwatt.

`plot` List all the probes for all modes.

`plot dc` Display the DC plot list.

`plot ac CLear` Clear the AC list.

2.35 PRINT command

2.35.1 Syntax

PRint
PRint *mode points ... ...*
PRint *mode + points ... ...*
PRint *mode - points ... ...*
PRint *mode* CLEAR

2.35.2 Purpose

Select points in the circuit for tabular output. Select tabular output.

2.35.3 Comments

The '`print`' command selects where to look at the circuit, or where to hook the voltmeter (ammeter, watt meter, ohm meter, etc.) probe.

There are separate lists of probe points for each type of analysis.

To list the probe points, use the bare command '`print`'.

On start-up, probes are not set. You must do the command '`print op v(nodes)`' or put '`.print op v(nodes)`' in the circuit file to get any output from the `op` command.

Syntax for each point is *parameter(node)*, *parameter(componentlabel)*, or *parameter(index)*. Some require a dummy index.

You can access components in subcircuits by connecting the names with dots. For example: `R56.X67.Xone` is `R56` in `X67` in `Xone`. Some built-in elements, including diodes, transistors, and mosfets, contain subcircuits with internal elements. `Cgd.M12` is the gate to drain capacitor of mosfet `M12`.

If the component does not exist, you will get an error message. If the component exists but the parameter is not valid for that type, there will be no error message but the value printed will be obviously bogus.

The options `plot` and `noplot` on any analysis command turn plotting on and off a single run. The `plot` command turns plotting on and tabular output off. The `print` command turns plotting off and tabular output on.

You can add to or delete from an existing list by prefixing with `+` or `-`. `print ac + v(3)` adds v(3) to the existing set of AC probes. `print ac - q(c5)` removes q(c5) from the list. You can use the wildcard characters `*` and `?` when deleting.

2.35.4 Node probes

Several parameters are available at each node.

All modes

`V` Voltage.

All except Transient

`Z` Impedance looking into the node.

Transient, DC, OP only

`Logic` A numeric interpretation of the logic value at the node. The value is displayed encoded in a number of the form *a.bc* where *a* is the logic state: 0 = logic 0, 1 = rising, 2 = falling, 3 = logic 1. *b* is an indication of the quality of the digital signal. 0 is a fully valid logic signal. Nonzero indicates it does not meet the criteria for logic simulation. *c* indicates how the node was calculated: 0 indicates logic simulation. 1 indicates analog simulation of a logic device. 2 indicates analog simulation of analog devices.

AC only

`VM` Voltage magnitude.

`VDB` Decibels relative to 1 volt.

`VP` Voltage phase.

`ZM` Port impedance magnitude.

`ZP` Port impedance phase. Negative phase is capacitive. Positive phase is inductive.

`ZR` Port impedance real part.

`ZI` Port impedance imaginary part.

2.35.5 Status probes

There are several status variables that can be probed.

All modes

`Temperature(0)` The simulation temperature in degrees Celsius.

`TIme(0)` The current time in a transient analysis. In AC analysis it shows the time at which the bias point was set, 0 if it was set in a DC or OP analysis, or -1 if it is the bias was not set (power off).

Transient, DC, OP only

`GEnerator` The output of the "signal generator". In a transient analysis, it shows the output of the signal generator, as set up by the `generator` command. In a DC analysis, it shows the DC input voltage (not the power supply). In an OP analysis, it shows the DC input, normally zero.

`ITer(0)` The number of iterations needed for convergence for this printed step including any hidden steps.

`ITer(1)` The number of iterations needed for convergence for this printed step not including any hidden steps.

`ITer(2)` The total number of iterations needed since startup including check passes.

`Control(0)` A number indicating why the simulator chose this time to simulate at.

1 The user requested it. One of the steps in a sweep.

2 A discrete event. An element required a solution at this time.

3 The effect of the "`skip`" parameter.

4 The iteration count exceeded `ITL4` so the last step was rejected and is being redone at a smaller time step.

5 The iteration count exceeded `ITL3` so the time interval is the same as it was last time.

6 Determined by local truncation error or some other device dependent approximation in hopes of controlling accuracy.

7,8 The step size was limited to twice the previous step size.

9 The step size was reduced to half the interval to an event to avoid a tiny next step.

10 + x The previous step was rejected.

20 + x A zero time step was replaced by *mrt*.

30 + x The required step size less than *mrt*, so it was replaced by *mrt*.

`Control(1)` The number internal time steps. (1 if all steps are printed. One more than the number of hidden steps.)

2.35.6 Element probes

Each element type has several parameters that can be probed. In general, the form is `Parameter(element)`. Wild cards are allowed in element names to allow probing the same parameter of a group of elements.

For components in a subcircuit, the names are connected with dots. For example `R12.X13` is `R12` in the subcircuit `X13`.

Most two node elements (capacitors, inductors, resistors, sources) have at least the following parameters available. Others are available for some elements.

All modes

`V` Branch voltage. The first node in the net list is assumed positive.

`I` Branch current. It flows into the first node in the net list, out of the second.

`P` Branch power. Positive power indicates dissipation. Negative power indicates that the part is supplying power. Its value is the same as (PD - PS). In AC analysis, it is the real part only.

`EV` The effective value of the part, in its units. If the part is ordinary, it will just show its value, but if it is time variant or nonlinear, it shows what it is now.

`R` Resistance. The effective resistance of the part, in ohms. In AC analysis, shows the magnitude of the self impedance. In `OP`, `DC` or `TRansient` analysis, shows its incremental resistance. In `TRansient` analysis, it shows the effective Z-domain resistance of inductors and capacitors.

`Y` Admittance.

All except Transient

Z Impedance at a port. The port impedance seen looking into the circuit across the branch. It does not include the part itself. In transient analysis, it shows the effective Z-domain impedance, which is a meaningless number if there are capacitors or inductors in the circuit.

Transient, DC, OP only

These parameters are available in addition to the above.

PD Branch power dissipated. The power dissipated in the part. It is always positive and does not include power sourced.

PS Branch power sourced. The power sourced by the part. It is always positive and does not consider its own dissipation.

F The result of evaluating the function related to the part. It is the voltage across a resistor, the charge stored in a capacitor, the flux in an inductor, etc.

AC only

These parameters are available in addition to the above.

VM Voltage magnitude.

VDB Decibels relative to 1 volt.

VP Voltage phase.

IM Current magnitude.

IDB Decibels relative to 1 amp.

IP Current phase.

P Real power.

PDB Decibels relative to 1 watt real power.

PX Reactive (imaginary) power, volt-amps reactive.

PXDB Decibels relative to 1 va reactive.

PM Volt amps, complex power.

PMDB Decibels relative to 1 va.

PP Power phase (angle between voltage and current). Negative phase is capacitive. Positive phase is inductive.

PF Power factor (cosine of power phase).

RM Self impedance magnitude.

RP Self impedance phase. Negative phase is capacitive. Positive phase is inductive.

RR Resistance, self impedance real part.

RI Reactance, self impedance imaginary part.

YM Self admittance magnitude.

YP Self admittance phase. Negative phase is capacitive. Positive phase is inductive.

YR Conductance, self admittance real part.

YI Self admittance imaginary part.

ZM Port impedance magnitude.

ZP Port impedance phase. Negative phase is capacitive. Positive phase is inductive.

ZR Port impedance real part.

ZI Port impedance imaginary part.

2.35.7 Examples

`print ac v(12) v(13) v(14)` The voltage at nodes 12, 13, and 14 for AC analysis.

`print dc v(r26)` The voltage across `R26`, for DC analysis.

`print tran v(r83) p(r83)` Voltage and power of `R83`, for transient analysis.

`print dc i(c8) p(r5) z(r5)` The current through `C8`, power dissipated in `R5`, and the impedance seen looking into the circuit across `R5`.

`print op v(nodes)` The voltage at all nodes for the `op` command.

`print` List all the probes, for all modes.

`print op` Display the `OP` probe list.

`print ac clear` Clear the AC list.

2.36 QUIT command

2.36.1 Syntax

`Quit`

2.36.2 Purpose

Terminates the program.

2.36.3 Comments

'`exit`' also works.

Be sure you have saved everything you want to!

2.37 SAVE command

2.37.1 Syntax

`SAve` *filename* {*options ...*}

2.37.2 Purpose

Saves the circuit on the disk.

2.37.3 Comments

The file is in an ASCII format, so the list may be used as part of a report. It is believed to be compatible with other simulators such as Berkeley Spice to the extent that the capabilities are the same. Compatibility with commercial Spice derivatives may be a problem because they all have proprietary extensions and are incompatible with each other.

If the file name specified already exists, the old file is deleted and replaced by a new file of the same name, after asking you for permission.

You can save a part of a circuit. See the `list` command for more details.

2.37.4 Examples

`save works.ckt` Save the circuit in the file `works.ckt`, in the current directory.

`save` Save the circuit. Since you did not specify a file name, it will ask for one.

`save partof.ckt R*` Save a partial circuit, just the resistors, to the file `partof.ckt`. (See the `List` command.)

`save /client/sim/ckt/no33` You can specify a path name.

2.38 SENS command

The Spice `SENS` command is not implemented. Similar functionality is not available.

2.39 STATUS command

2.39.1 Syntax

`STatus`

2.39.2 Purpose

Shows information on how the system resources are being utilized.

2.40 SWEEP command

2.40.1 Syntax

`SWeep` {*stepcount*} *partlabel=range ...*

2.40.2 Purpose

Sweep a component (or group of components) over a range. Set up a loop for iteration.

2.40.3 Comments

This command begins a loop which will sweep a component or group of components.

When this command is given, the only apparent actions will be a change in the prompt from '`-->`' to '`>>>`', and some disk action.

The different prompt means that commands are not executed immediately, but are stored in a temporary file.

The bare command will repeat the same command sequence as the last time `SWeep` was run, and not prompt for anything else.

Additional components can be swept at the same time by entering a '`FAult`' command at the '`>>>`' prompt. The '`FAult`' behaves differently here: It accepts a range, which is the sweep limits.

The '`GO`' command will end the entry sequence, and make it all happen. After this, the values are restored. (Also, all `FAult`s are restored, as if by the '`Restore`' command.)

All commands can be used in this mode. Of course, some of them are not really useful (`Quit`) because they work as usual.

Only linear, ordinary parts can be swept. (No semiconductor devices, or elements using behavioral modeling.) The tolerance remains unchanged. If you attempt to sweep a nonlinear or otherwise strange part, it becomes ordinary and linear during the sweep.

2.40.4 Example

```
-->sweep  5   R14=1,100k   R15=100k,1
>>>list
>>>ac 500 2k oct
>>>go
```

This sequence of commands says to simultaneously sweep R14 and R15 in 5 steps, in opposite directions, list the circuit and do an AC analysis for each step.

Assuming the circuit was:

```
R14  1   0   50k
R15  2   0   50k
```

The result of this sequence would be:

```
R14  1   0   1
R15  2   0   100k
```

an AC analysis

```
R14  1   0   25.75k
R15  2   0   75.25k
```

an AC analysis

```
R14  1   0   50.5k
R15  2   0   50.5k
```

an AC analysis

```
R14  1   0   75.25k
R15  2   0   25.75k
```

an AC analysis

```
R14  1   0   100k
R15  2   0   1
```

an AC analysis

After all this is done, the circuit is restored, so `list` would show:

```
R14  1   0   50k
R15  2   0   50k
```

You could accomplish the same thing by entering `fault` commands at the '`>>>`' prompt.

```
-->sweep  5
>>>fault  R14=1, 100k
>>>fault  R15=100k, 1
>>>list
>>>ac 500 2k oct
>>>go
```

2.41 TEMP command

The Spice `TEmp` command is not implemented. Similar functionality is available by sweeping the `op` command.

2.42 TF command

The Spice `TF` command is not implemented. Similar functionality is not available.

2.43 TITLE command

2.43.1 Syntax

```
TItle
TItle a line of text
```

2.43.2 Purpose

View and create the heading line for printouts and files.

2.43.3 Comments

There is a header line at the beginning of every file, to help you identify it in the future. This command sets up what it says. It also sets up a heading for printouts and graphs.

When you use the '`get`' command to bring in a new circuit, it replaces the title with the one in the file. The '`title`' command lets you change it, for the next time it is written out.

2.43.4 Examples

`title This is a test.` Sets the file heading to '`This is a test.`' In the future, all files written will have '`This is a test.`' as their first line.

`title` Displays the file heading. In this case, it prints '`This is a test.`'

2.44 `TRANSIENT` command

2.44.1 Syntax

`Transient` *start stop stepsize* {*options ...*}
`Transient` *stepsize stop start* {*options ...*}

2.44.2 Purpose

Performs a nonlinear time domain (transient) analysis.

2.44.3 Comments

The nodes to look at must have been previously selected by the `Print` or `Plot` command.

Three parameters are normally needed for a Transient analysis: start time, stop time and step size, in this order. The SPICE order (step size, stop, start) is also acceptable. An optional fourth parameter is the maximum internal time step.

If all of these are omitted, the simulation will continue from where the most recent one left off, with the same step size, unless the circuit topology has been changed. It will run for the same length of time as the previous run.

Do not use a step size too large as this will result in errors in the results. If you suspect that the results are not accurate, try a larger argument to 'Skip'. This will force a smaller internal step size. If the results are close to the same, they can be trusted. If not, try a still larger 'Skip' argument until they appear to match close enough.

The most obvious error of this type is aliasing. You must select sample frequency at least twice the highest signal frequency that exists anywhere in the circuit. This frequency can be very high, when you use the default step function as input. The signal generator does **not** have any filtering.

2.44.4 Options

`>` *file* Send results of analysis to *file*.

`>>` *file* Append results to *file*.

`Cold` Zero initial conditions. Cold start from power-up.

`DTMIn` $= x$ Minimum time step. (Default = from `options`) The smallest internal time step in transient analysis. The `transient` command `dtmin` option and the `dtratio` option override it if it is bigger.

`DTRatio` $= x$ The ratio between minimum and maximum time step. (Default = from `options`).

`NOPlot` Suppress plotting.

`PLot` Graphic output, when plotting is otherwise off.

`Quiet` Suppress console output.

`Skip` *count* Force at least *count* simulation steps for each one displayed. If the output is a table or ASCII plot, the extra steps are hidden.

`TEmperature` *degrees* Temperature, degrees C.

`TRace` n Show extended information during solution. Must be followed by one of the following:

- `Off` No extended trace information (default, override .opt)
- `Warnings` Show extended warnings
- `Alltime` Show all accepted internal time steps.
- `Rejected` Show all internal time steps including rejected steps.

`Iterations` Show every iteration.

`Verbose` Show extended diagnostics.

`UIC` Use initial conditions. ACS will use the values specified with the `IC =` options on the various elements.

2.44.5 Examples

`transient 0 100u 10n` Start at time 0, stop after 100 micro-seconds. Simulate using 10 nanosecond steps.

`transient` No parameters mean to continue from the last run. In this case it means to step from 100 us to 200 us in 10 ns steps. (The same step size and run length, but offset to start where the last one stopped.

`transient skip 10` Do 10 extra steps internally for every step that would be done otherwise. In this case it means to internally step at 1 nanosecond. If the output is in tabular form, the extra steps are hidden.

`transient 0` Start over at time = 0. Keep the same step size and run length.

`transient cold` Zero initial conditions. This will show the power-on transient.

`transient >arun` Save the results of this run in the file `arun`.

2.45 UNFAULT command

2.45.1 Syntax

`UNFault`

2.45.2 Purpose

Undo any action from `fault` commands.

2.45.3 Comments

This command reverses the action of all `fault` commands.

It will also clean up any side effects of an aborted `sweep` command.

`Unfault` is automatically invoked on any `clear` command.

If you change the circuit in any other way, `unfault` will bring back the old on top of the changes. This can bring on some surprises.

2.45.4 Example

`fault R66=1k` R66 now has a value of 1k, regardless of what it was before.

`unfault` Clears all faults. In this case, R66 has its old value again.

`unfault` can bring on surprises. Consider this sequence ...

```
V1   1   0    ac  1
C3   1   2    1u
R4   2   0    10k
```

`fault C3=100p` C3 is 100 picofarads, for now.

`modify C3=220p` C3 is 220 pf, for now. It will be restored.

`modify R4=1k` R4 is 1k. It will not be restored.

`restore` C3 back to 1 uf, but R4 still 1k.

2.46 UNMARK command

2.46.1 Syntax

`UNMark`

2.46.2 Purpose

Forget remembered circuit voltages and currents. Undo the '`mark`' command.

2.46.3 Comments

Allow time to proceed. It has been held back by the '`mark`' command.

2.46.4 Examples

`transient 0 1 .01` A transient analysis starting at zero, running until 1 second, with step size .01 seconds. After this run, the clock is at 1 second.

`mark` Remember the time, voltages, currents, etc.

`transient` Another transient analysis. It continues from 1 second, to 2 seconds. (It spans 1 second, as before.) This command was not affected by the `mark` command.

`transient` This will do exactly the same as the last one. From 1 second to 2 seconds. If it were not for `mark`, it would have started from 2 seconds.

`transient 1.5 .001` Try again with smaller steps. Again, it starts at 1 second.

`unmark` Release the effect of `mark`.

`transient` Exactly the same as the last time, as if we didn't `unmark`. (1 to 1.5 seconds.)

`transient` This one continues from where the last one left off: at 1.5 seconds. From now on, time will move forward.

2.47 `WIDTH` command

2.47.1 Syntax

`Width` {`IN=`*value*} {`OUT=`*value*}

2.47.2 Purpose

Set input and output width.

2.47.3 Comments

The '`width`' command is the same as the '`options`' command. It is provided for SPICE compatibility. SPICE uses `width` to set two parameters: `in` and `out`, which we set with the `options` command.

Chapter 3

Circuit description

3.1 Summary

To describe a circuit, you must provide a 'netlist'. The netlist is simply a list of the components with their connections and values. The format is essentially the same as the standard SPICE format.

Before doing this, number the nodes on your schematic. (A node is a place where parts connect together.) Then, each part gets a line in the netlist (circuit description). In its simplest form, which you will use most of the time, it is just the type, such as 'R' for resistor, or a label, like 'R47', followed by the two nodes it connects to, then its value.

Example: '`R29 6 8 22k`' is a 22k resistor between nodes 6 and 8.

Node 0 is used as a reference for all calculations and is assumed to have a voltage of zero. (This is the ground, earth or common node.) Nodes must be nonnegative integers, but need not be numbered sequentially.

There should be a DC path through the circuit to node 0 from every node that is actually used. The circuit cannot contain a cutset of current sources and/or capacitors. If either of these cases occurs, it will be discovered during analysis. The program will attempt to correct the error, issue an 'open circuit' error message and continue. This is rarely a problem with real circuits. Most circuits have such a path, however indirect.

Semiconductor devices require both a device statement, and a `.model` statement (or "card"). The device statement, described in the Circuit description chapter, defines individual devices as variations from a prototype, as is required for different devices on the same substrate. The model statement, described in this chapter, defines process dependent parameters, which usually apply to all devices on a substrate.

The `.model` card syntax is:

`.model` *mname type* {*args*}

Mname is the model name, which elements will use to refer to this model. *Type* is one of several types of built-in models. *Args* is a list of the parameters, of the form *name*=*value*.

`D` Diode model

`NMOS` N-channel MOSFET model

`PMOS` P-channel MOSFET model

`LOGIC` Logic family description

`SW` Voltage controlled switch

`CSW` Current controlled switch

3.2 `C`: Capacitor

3.2.1 Syntax

`C`*xxxxxxx n+ n– value*
`C`*xxxxxxx n+ n– expression*
`C`*xxxxxxx n+ n– value* {`IV=`*initial-voltage*}
`.CAPacitor` *label n+ n– expression*

3.2.2 Purpose

Capacitor, or general charge storage element.

3.2.3 Comments

N+ and *n–* are the positive and negative element nodes, respectively. *Value* is the capacitance in Farads.

The (optional) initial condition is the initial (time = 0) value of the capacitor voltage (in Volts). Note that the initial conditions (if any) apply only if the `UIC` option is specified on the `transient` command.

3.3 Trans-capacitor

3.3.1 Syntax

`.TCAPacitor` *label n+ n– nc+ nc– expression* `.TCAPacitor` *label n+ n– nc+ nc– value* {`IV=`*initial-voltage*}

3.3.2 Purpose

Trans-capacitor, or charge transfer device.

3.3.3 Comments

N+ and *n–* are the positive and negative element nodes, respectively. *Nc+* and *nc–* are the positive and negative controlling nodes, respectively. *Expression* is the capacitance in Farads.

The (optional) initial condition is the initial (time = 0) value of the capacitor voltage (in Volts). Note that the initial conditions (if any) apply only if the `UIC` option is specified on the `transient` command.

This device places a charge between the output nodes that depends on the voltage on its input nodes. If you parallel the input with the output, it becomes an ordinary capacitor. While the use of this device may appear straightforward, be careful. It is easy to use it in an unstable way.

It is used internally in some transistor models.

3.4 `D`: Diode

3.4.1 Syntax

`D`*xxxxxxx n+ n– mname* {*area*} {*args*}
`.DIOde` *xxxxxxx n+ n– mname* {*area*} {*args*}

3.4.2 Purpose

Junction diode.

3.4.3 Comments

N+ and *n–* are the positive and negative element nodes, respectively. *Mname* is the model name. *Area* is the area factor. If the area factor is omitted, a value of 1.0 is assumed. *Args* is a list of additional arguments. The parameters available are a superset of those available in SPICE.

A diode can also use a MOSFET model (type `NMOS` or `PMOS`) to represent the equivalent of the source-bulk or drain-bulk diodes.

When the element is printed out, by a `list` or `save` command, the the computed values of `IS`, `RS`, `CJ`, and `CJSW` are printed as a comment if they were not explicitly entered.

3.4.4 Element Parameters

`Area` = *x* Area factor. (Default = 1.0) If optional parameters `IS`, `RS`, and `CJO` are not specified, the `.model` value is multiplied by `area` to get the actual value.

`Perim` = *x* Perimeter factor. (Default = 1.0) If optional parameter `CJSW` is not specified, the `.model` value is multiplied by `perim` to get the actual value.

`IC` = *x* Initial condition. The initial voltage to use in transient analysis, if the `UIC` option is specified. Default: don't use initial condition. This is presently ignored, but accepted for compatibility.

`OFF` Start iterating with this diode off, in DC analysis.

`STIFF` Use a stiffly stable integration method and ignore truncation error.

`IS` = *x* Saturation current. This overrides `IS` in the `.model`, and is not affected by `area`. Default: use `IS` from `.model` * `area`.

`RS` = *x* Ohmic (series) resistance. This overrides `RS` in the `.model`, and is not affected by `area`. Default: use `RS` from `.model` * `area`. This is presently ignored, but accepted for compatibility.

CJ = x Zero-bias junction capacitance. This overrides CJ in the .model, and is not affected by area. Default: use CJ from .model * area.

CJSW = x Zero-bias sidewall capacitance. This overrides CJSW in the .model, and is not affected by perim. Default: use CJSW from .model * perim.

3.4.5 Model Parameters

IS = x Normalized saturation current. (Amperes). (Default = 1.0e-14) IS is multiplied by the *area* in the element statement to get the actual saturation current. It may be overridden by specifying IS in the element statement.

RS = x Normalized ohmic resistance. (Ohms) (Default = 0.) RS is multiplied by the *area* in the element statement to get the actual ohmic resistance. It may be overridden by specifying RS in the element statement. RS is accepted, and silently ignored, for compatibility, but not implemented.

N = x Emission coefficient. (Default = 1.0) In ECA-2 the default value was 2.

TT = x Transit time. (Default = 0.) The diffusion capacitance is given by: $c_d = TTg_d$ where g_d is the diode conductance.

VJ = x Junction potential. (Default = 1.0) Used in computation of capacitance. For compatibility with older versions of SPICE, PB is accepted as an alias for VJ.

CJo = x Normalized zero-bias depletion capacitance. (Default = 0.) CJo is multiplied by the *area* in the element statement to get the actual zero-bias capacitance. It may be overridden by specifying CJ in the element statement.

Mj = x Grading coefficient. (Default = 0.5)

PBSw = x Sidewall junction potential. (Default = PB)

CJSw = x Normalized zero-bias sidewall capacitance. (Default = 0.) CJSw is multiplied by the *perimeter* in the element statement to get the actual zero-bias capacitance. It may be overridden by specifying CJSW in the element statement.

MJSw = x Sidewall grading coefficient. (Default = 0.33)

EG = x Activation energy. (electron Volts) (Default = 1.11, silicon.) For other types of diodes, use:

1.11 ev. Silicon (default value)
0.69 ev. Schottky barrier
0.67 ev. Germanium
1.43 ev. GaAs
2.26 ev. GaP

XTI = x Saturation current temperature exponent. (Default = 3.0) For Schottky barrier, use 2.0.

KF = x Flicker noise coefficient. (Default = 0.) SPICE parameter accepted but not implemented.

AF = x Flicker noise exponent. (Default = 1.0) SPICE parameter accepted but not implemented.

FC = x Coefficient for forward bias depletion capacitance formula. (Default = 0.5)

BV = x Reverse breakdown voltage. (Default = ∞.) SPICE parameter accepted but not implemented.

IBV = x Current at breakdown voltage. (Default = 1 ma.) SPICE parameter accepted but not implemented.

STIFF Use a stiffly stable integration method and ignore truncation error.

3.4.6 Probes

Vd Voltage. The first node (anode) is assumed positive.

Id Total current. It flows into the first node (anode), out of the second (cathode). I(Dxxxx) is the same as IJ(Dxxxx) + IC(Dxxxx).

IJ Junction current. The current through the junction. IJ(Dxxxx) is the same as I(Yj.Dxxxx).

IC Capacitor current. The current through the parallel capacitor. IC(Dxxxx) is the same as I(Cj.Dxxxx).

`P` Power. P(Dxxxx) is the same as PJ(Dxxxx) + PC(Dxxxx).

`PD` Power dissipated. The power dissipated as heat. It is always positive and does not include power sourced. It should be the same as P because the diode is passive.

`PS` Power sourced. The power sourced by the part. It is always positive and does not consider its own dissipation. It should be 0 because the diode is passive.

`PJ` Junction power. PJ(Dxxxx) is the same as P(Yj.Dxxxx).

`PC` Capacitor power. PC(Dxxxx) is the same as P(Cj.Dxxxx).

`Cap` Effective capacitance. C(Dxxxx) is the same as EV(Cj.Dxxxx).

`Req` Effective resistance. R(Dxxxx) is the same as R(Yj.Dxxxx).

`REgion` Region code. A numeric code that represents the region it is operating in. +1 = forward, -1 = reversed, 0 = unknown.

All parameters of the internal elements Yj and Cj are available. To access them, concatenate the labels for the internal element with the diode, separated by a dot. Yj.D6 is the admittance (Yj) element of the diode D6.

In this release, there are no probes available in AC analysis except for the internal elements.

3.5 E: Voltage Controlled Voltage Source

3.5.1 Syntax

E*xxxxxxx n+ n– nc+ nc– value*
E*xxxxxxx n+ n– nc+ nc– expression*
`.VCVS` *label n+ n– nc+ nc– expression*

3.5.2 Purpose

Voltage controlled voltage source, or voltage gain block.

3.5.3 Comments

N+ and *n–* are the positive and negative element (output) nodes, respectively. *Nc+* and *nc–* are the positive and negative controlling nodes, respectively. *Value* is the voltage gain.

3.6 F: Current Controlled Current Source

3.6.1 Syntax

F*xxxxxxx n+ n– ce value*
F*xxxxxxx n+ n– ce expression*
`.CCCS` *label n+ n– ce expression*

3.6.2 Purpose

Current controlled current source, or current gain block.

3.6.3 Comments

N+ and *n–* are the positive and negative element (output) nodes, respectively. Current flow is from the positive node, through the source, to the negative node. *Ce* is the name of an element through which the controlling current flows. The direction of positive controlling current is from the positive node, through the element, to the negative node of *ce*. *Value* is the transconductance in mhos.

The controlling element can be any simple two terminal element. Unlike SPICE, it does not need to be a voltage source.

3.7 G: Voltage Controlled Current Source

3.7.1 Syntax

G*xxxxxxx n+ n– nc+ nc– value*
G*xxxxxxx n+ n– nc+ nc– expression*
`.VCCS` *label n+ n– nc+ nc– expression*

3.7.2 Purpose

Voltage controlled current source, or transconductance block.

3.7.3 Comments

N+ and *n–* are the positive and negative element (output) nodes, respectively. Current flow is from the positive node, through the source, to the negative node. *Nc+* and *nc–* are the positive and negative controlling nodes, respectively. *Value* is the transconductance in mhos.

3.8 Voltage Controlled Capacitor

3.8.1 Syntax

Preferred syntax:
`.VCCAP` *label n+ n– nc+ nc– expression*
Alternate syntax (HSpice style)
`G`*xxxxxxx n+ n–* VCCAP *nc+ nc– expression*

3.8.2 Purpose

Voltage controlled capacitor.

3.8.3 Comments

N+ and *n–* are the positive and negative element (output) nodes, respectively. *Nc+* and *nc–* are the positive and negative controlling nodes, respectively. *Value* is the transfactor in Farads per volt.

The simulator will faithfully give you a negative capacitor if it seems appropriate. Usually, this part is used with a behavioral modeling function, like PWL, which allows you to specify a table of capacitance vs. voltage.

3.9 Voltage Controlled Admittance

3.9.1 Syntax

Preferred syntax:
`.VCG` *label n+ n– nc+ nc– expression*
Alternate syntax (HSpice style)
`G`*xxxxxxx n+ n–* VCG *nc+ nc– expression*

3.9.2 Purpose

Voltage controlled admittance.

3.9.3 Comments

N+ and *n–* are the positive and negative element (output) nodes, respectively. *Nc+* and *nc–* are the positive and negative controlling nodes, respectively. *Value* is the transfactor in mhos per volt.

The simulator will faithfully give you a negative admittance if it seems appropriate. Usually, this part is used with a behavioral modeling function, like PWL, which allows you to specify a table of admittance vs. voltage.

3.10 Voltage Controlled Resistor

3.10.1 Syntax

Preferred syntax:
`.VCR` *label n+ n– nc+ nc– expression*
Alternate syntax (HSpice style)
`G`*xxxxxxx n+ n–* VCR *nc+ nc– expression*

3.10.2 Purpose

Voltage controlled resistor.

3.10.3 Comments

N+ and *n–* are the positive and negative element (output) nodes, respectively. *Nc+* and *nc–* are the positive and negative controlling nodes, respectively. *Value* is the transfactor in ohms per volt.

The simulator will faithfully give you a negative resistor if it seems appropriate. Usually, this part is used with a behavioral modeling function, like PWL, which allows you to specify a table of resistance vs. voltage.

3.11 H: Current Controlled Voltage Source

3.11.1 Syntax

H*xxxxxxx n+ n– ce value*
H*xxxxxxx n+ n– ce expression*
.CCVS *label n+ n– ce expression*

3.11.2 Purpose

Current controlled voltage source, or transresistance block.

3.11.3 Comments

N+ and *n–* are the positive and negative element (output) nodes, respectively. *Ce* is the name of an element through which the controlling current flows. The direction of positive controlling current is from the positive node, through the element, to the negative node of *ce*. *Value* is the transresistance in Ohms.

The controlling element can be any simple two terminal element. Unlike SPICE, it does not need to be a voltage source.

3.12 I: Independent Current Source

3.12.1 Syntax

I*xxxxxxx n+ n– value*
I*xxxxxxx n+ n– expression*
.ISOurce *label n+ n– expression*

3.12.2 Purpose

Independent current source.

3.12.3 Comments

N+ and *n–* are the positive and negative element nodes, respectively. Positive current flow is from the positive node, through the source, to the negative node. *Value* is the current in Amperes.

All of the SPICE time dependent functions (`pulse`, `sin`, `exp`, `pwl`, and `sffm` are supported. An additional function `generator` emulates a laboratory type function generator, for a more convenient signal input to the circuit.

3.13 J: Junction Field-Effect Transistor

3.13.1 Syntax

J*xxxxxxx nd ng ns mname* {*area*} {*args*}

3.13.2 Purpose

Junction Field Effect Transistor.

3.13.3 Comments

Not implemented. Plans are to implement it as in SPICE.

3.14 K: Coupled (Mutual) Inductors

3.14.1 Syntax

K*xxxxxxx* L*yyyyyyy* L*zzzzzzz value*
.MUTual_inductor *label* L*yyyyyyy* L*zzzzzzz value*

3.14.2 Purpose

Coupled mutual inductance.

3.14.3 Comments

K couples two inductors. The value is the coefficient of coupling. Using the dot convention, place a dot on the first node of each inductor.

The coefficient of coupling is given by $K = \frac{M_{ij}}{\sqrt{L_i L_j}}$.

3.14.4 Bugs

This release does not support multiple coupled inductors.

3.15 L: Inductor

3.15.1 Syntax

L*xxxxxx n+ n– value*
L*xxxxxx n+ n– expression*
L*xxxxxx n+ n– value* {II=*initial-current*}
.INDuctor *label n+ n– expression*

3.15.2 Purpose

Inductor, or general flux storage element.

3.15.3 Comments

N+ and *n–* are the positive and negative element nodes, respectively. *Value* is the inductance in Henries.

The (optional) initial condition is the initial (time = 0) value of the inductor current (in Amperes). Note that the initial conditions (if any) apply only if the UIC option is specified on the transient command.

3.16 M: MOSFET

3.16.1 Syntax

M*xxxxxxx nd ng ns nb mname* {*args*}
M*xxxxxx nd ng ns nb mname* {*width/length*} {*args*}
.MOSfet *label nd ng ns nb mname* {*args*}
.MOSfet *label nd ng ns nb mname* {*width/length*} {*args*}

3.16.2 Purpose

MOSFET.

3.16.3 Comments

Nd, *ng*, *ns*, and *nb* are the drain, gate, source, and bulk (substrate) nodes, respectively. *Mname* is the model name.

Length and *width* are the drawn channel length and width, in microns. Note that the notation W/L has units of microns, but the same parameters, in the argument list (W and L) have units of meters. All other dimensions are in meters.

The options rstray and norstray determines whether or not series resistances are included. Experience has shown that the effect of series resistance is usually not significant, it can significantly degrade the simulation time, and it often increases roundoff errors. Therefore, norstray is the default. Norstray is the equivalent of setting the model parameters rd, rs, and rsh all to zero.

Entering a parameter value of 0 is not the same as not specifying it. This behavior is not compatible with SPICE. In SPICE, a value of 0 is often interpreted as not specified, with the result being to calculate it some other way. If you want it to be calculated, don't specify it.

Another subtle difference from SPICE is that ACS may omit some unnecessary parts of the model, which may affect some reported values. It should not affect any voltages or currents. For example, if the gate and drain are tied, Cgs will be omitted from the model, so the printed value for Cgdovl and Cgd will be 0, which will disagree with SPICE. It doesn't matter because a shorted capacitor can store no charge.

Levels 1, 2, 3, 4, 5, 6 are implemented.

3.16.4 Element Parameters

Basic Spice compatible parameters

L = *x* Drawn channel length. (Default = DEFL parameter from options. DEFL default = 100μ)

W = *x* Drawn channel width. (Default = DEFW parameter from options. DEFW default = 100μ)

AD = *x* Area of drain diffusion. (Default = DEFAD parameter from options. DEFAD default = 0)

AS = *x* Area of source diffusion. (Default = DEFAS parameter from options. DEFAS default = 0)

PD = *x* Perimeter of drain junction. (Default = 0.)

PS = *x* Perimeter of source junction. (Default = 0.)

NRD = *x* Number of squares of drain diffusion. (Default = 1.)

NRS = *x* Number of squares of source diffusion. (Default = 1.)

3.16.5 Model Parameters

Basic selection – required for all models

`LEVEL` = x Model index. (Default = 1) Selects which of several models to use. The choices supported are 1, 2, 3, and 6, corresponding to Spice 3f.

Substrate coupling – all models

`IS` = x Bulk junction saturation current. If not input, it is calculated from `JS`. If both are input, a warning is issued, and the calculated value (from `JS`) is used, if `AD` and `AS` are also input. If neither `IS` or `JS` is input, a default value of 1e-14 is used.

`JS` = x Bulk junction saturation current per sq-meter of junction area. May be used to calculate `IS`. If a conflict exists, a warning is issued.

`FC` = x Coefficient for forward bias depletion capacitance formula. (Default = 0.5)

`PB` = x Bulk junction potential. (Default = 0.8)

`CJ` = x Zero bias bulk junction bottom capacitance per sq-meter of junction area. If not input, but `NSUB` is, it is calculated, otherwise a default value of 0 is used.

`MJ` = x Bulk junction bottom grading coefficient. (Default = 0.5)

`PBSW` = x Sidewall Bulk junction potential. (Default = PB)

`CJSW` = x Zero bias bulk junction sidewall capacitance per meter of junction perimeter. (Default = 0.)

`MJSW` = x Bulk junction sidewall grading coefficient. (Default = 0.33)

Strays – all models

`RSH` = x Drain and source diffusion sheet resistance. If not input, use `RS` and `RD` directly. If a conflict exists, a warning is issued. The resistance is only used if the option `rstray` is set.

`RD` = x Drain ohmic resistance (unscaled). If `RS` is input, the default value of `RD` is 0. If `RD` and `RS` are both not input, and `RSH` is input, they are calculated from `RSH`. If any conflict exists, a warning is issued, indicating the action taken, which is believed to be compatible with SPICE. The resistance is only used if the option `rstray` is set.

`RS` = x Source ohmic resistance (unscaled). If `RD` is input, the default value of `RS` is 0. If `RD` and `RS` are both not input, and `RSH` is input, they are calculated from `RSH`. If any conflict exists, a warning is issued, indicating the action taken, which is believed to be compatible with SPICE. The resistance is only used if the option `rstray` is set.

`CBD` = x Zero bias B-D junction capacitance (unscaled). If `CBD` is not specified, it is calculated from `CJ`.

`CBS` = x Zero bias B-S junction capacitance (unscaled). If `CBS` is not specified, it is calculated from `CJ`.

`CGSO` = x Gate-source overlap capacitance, per channel width. (Default = 0.)

`CGDO` = x Gate-drain overlap capacitance, per channel width. (Default = 0.)

`CGBO` = x Gate-bulk overlap capacitance, per channel length. (Default = 0.)

Accepted and ignored – all models

`KF` = x Flicker noise coefficient. SPICE parameter accepted but not implemented.

`AF` = x Flicker noise exponent. SPICE parameter accepted but not implemented.

Level 1,2,3,6 shared parameters

`VTO` = x Zero bias threshold voltage. If not input, but `NSUB` is, it is calculated, otherwise a default value of 0 is used.

`KP` = x Transconductance parameter. If not input, it is calculated by `UO` * `COX`.

`GAMMA` = x Bulk threshold parameter. If not input, but `NSUB` is, it is calculated, otherwise a default value of 0 is used.

PHI = x Surface potential. If not input, but NSUB is, it is calculated, otherwise a default value of 0.6 is used. A warning is issued if the calculated value is less than 0.1, in which case 0.1 is used.

LAMBDA = x Channel length modulation. If not input, it is calculated dynamically during simulation. If the value input is larger than 0.2, a warning is issued, but no correction is made. (accepted but ignored for level 3)

TOX = x Oxide thickness. (meters) (Default = 1e-7)

NSUB = x Substrate doping. (atoms / cm^3) Used in calculation of VTO, GAMMA, PHI, and CJ. If not input, default values are used.

NSS = x Surface state density. (atoms / cm^2) (Default = 0.) Used, with NSUB in calculation of VTO.

XJ = x Metallurgical junction depth. (meters) Used to calculate short channel effects. If not input, do not model short channel effects, effectively defaults to 0.

LD = x Lateral diffusion. (Default = 0.) Effective channel length is reduced by 2 * LD.

UO = x Surface mobility. (cm^2/V-s) (Default = 600.)

DELTA = x Width effect on threshold voltage. (Default = 0.) (Level 2 and 3 only.)

TPG = x Type of gate material. (Default = 1.)

+1 opposite to substrate
–1 same as substrate
0 Aluminum

CMODEL = x Capacitance model selector (Default = 2 for level 1,2,3. Default = 3 for level 6.) The only valid values are 2 and 3. 2 selects Meyer capacitance calculations compatible with Spice 2. 3 selects campatibility with Spice 3.

Level 1

The Level 1 model has no additional parameters.

Level 2

NFS = x Fast surface state density. (atoms / cm^2) Used in modeling subthreshold effects. If not input, do not model subthreshold effects.

VMAX = x Maximum drift velocity of carriers. (m/s) Used in calculating vdsat, and lambda. If not input, use a different method. VMAX does not always work, if the method fails, the alternate method is used and the warning "Baum's theory rejected" is issued if the error threshold is set to debug or worse.

NEFF = x Total channel charge (fixed and mobile) coefficient. (Default = 1.) Used in internal calculation of lambda.

UCRIT = x Critical field for mobility degradation. (V/cm) (Default = 1e4)

UEXP = x Critical field exponent in mobility degradation. If not input, do not model mobility degradation, effectively defaulting to 0.

UTRA = x Transverse field coefficient. SPICE parameter accepted but not implemented. It is also not implemented in most versions of SPICE.

Level 3

NFS = x Fast surface state density. (atoms / cm^2) Same as Level 2.

VMAX = x Maximum drift velocity of carriers. (m/s) Used in calculating vdsat. If not input, use a different method.

THETA = x Mobility modulation.

ETA = x Static feedback.

KAPPA = x Saturation field vector.

Level 6

KV = x Saturation voltage factor.

NV = x Saturation voltage coeff.

KC = x Saturation current factor.

NC = x Saturation current coeff.

`NVTH` = x Threshold voltage coeff.

`PS` = x Sat. current modification par.

`GAMMA1` = x Bulk threshold parameter 1.

`SIGMA` = x Static feedback effect par.

`LAMBDA1` = x Channel length modulation param. 1.

Level 4, 5, 7, 8 (BSIM models) general comments

The BSIM models have additional parameters for length, width, and product (length * width) dependency. To get the name, prefix the listed parameter with L, W, or P, respectively. Spice supports the "P" parameter only for BSIM3, but ACS supports it for all 3 models. For example, VFB is the basic parameter with units of Volts, and LVFB, WVFB, and PVFB also exist. The units of LVFB and WVFB are Volts * micron. The units of PVFB are Volts * micron * micron. The real parameter is calculated by $P = P_0 + P_L/L + P_W/W + P_P/(L*W)$, where L and W are the effective length and width in microns.

Level 4, "BSIM1"

undocumented

Level 5, "BSIM2"

undocumented

Level 7, "BSIM3v3.1"

not yet

Level 8, "BSIM3v3.2"

not yet

3.16.6 Probes

`VDS` Drain-source voltage.

`VGS` Gate-source voltage.

`VBS` Bulk-source voltage.

`VGD` Gate-drain voltage.

`VBD` Bulk-drain voltage.

`VSD` Source-drain voltage.

`VDG` Drain-gate voltage.

`VBG` Bulk-gate voltage.

`VSG` Source-gate voltage.

`VDB` Drain-bulk voltage.

`VGB` Gate-bulk voltage.

`VSB` Source-bulk voltage.

`VD` Drain-ground voltage.

`VG` Gate-ground voltage.

`VB` Bulk-ground voltage.

`VS` Source-ground voltage.

`Id` Drain current.

`IS` Source current.

`IG` Gate current.

`IB` Bulk current.

`CGSO` Gate-source overlap capacitance.

`CGDO` Gate-drain overlap capacitance.

`CGBO` Gate-bulk overlap capacitance.

`CGSm` Gate-source Meyer capacitance.

`CGDm` Gate-drain Meyer capacitance.

`CGBm` Gate-bulk Meyer capacitance.

`CGST` Gate-source total capacitance.

`CGDT` Gate-drain total capacitance.

`CGBT` Gate-bulk total capacitance.

`CBD` Bulk-drain junction capacitance.

`CBS` Bulk-source junction capacitance.

`CGATE` Nominal gate capacitance.

`GM` Transconductance.

`GDS` Drain-source conductance.

GMB Body effect transconductance.

VDSAT Saturation voltage.

VTH Threshold voltage.

IDS Drain-source current, not including strays.

IDSTray Drain current due to strays.

IError Estimated drain current error bound.

P Power dissipation.

P Power.

PD Power dissipated. The power dissipated as heat. It is always positive and does not include power sourced. It should be the same as P because the mosfet cannot generate energy.

PS Power sourced. The power sourced by the part. It is always positive and does not consider its own dissipation. It should be 0 because the mosfet cannot generate energy.

REgion Region code. A numeric code that represents the region it is operating in. The number is the sum of several factors. A negative code indicates the source and drain are reversed.

1 Active. (Not cut off.)

2 Not subthreshold.

4 Saturated.

10 Source to bulk is forward biased.

20 Drain to bulk is forward biased.

40 Punch through.

All parameters of the internal elements (Ids, Gmr, Gmf, Yds, Gmbr, Gmbf, Cgb, Cgd, Cgs, Dsb, Ddb, Rd, Rs) are available. To access them, concatenate the labels for the internal element with the diode, separated by a dot. Cgd.M6 is the gate to drain capacitance of M6.

In this release, there are no probes available in AC analysis except for the internal elements.

3.17 Q: Bipolar Junction Transistor

3.17.1 Syntax

Q*xxxxxxx nc nb ne mname* {*area*} {*args*}

3.17.2 Purpose

Bipolar junction transistor,

3.17.3 Comments

Not implemented. Plans are to implement it as in SPICE.

3.18 R: Resistor

3.18.1 Syntax

R*xxxxxxx n+ n– value*
R*xxxxxxx n+ n– expression*
.RESistor *label n+ n– expression*

3.18.2 Purpose

Resistor, or general current controlled dissipative element.

3.18.3 Comments

N+ and *n–* are the positive and negative element nodes, respectively. *Value* is the resistance in Ohms.

The resistor (type R) differs from the admittance (type Y) in that the resistor is a current controlled element, and the conductance is a voltage controlled element, in addition to the obvious use of conductance ($1/R$) instead of resistance.

3.19 S: Voltage Controlled Switch

3.19.1 Syntax

S*xxxxxxx n+ n– nc+ nc– mname* {*ic*}
.VSWitch *label n+ n– nc+ nc– mname* {*ic*}

3.19.2 Purpose

Voltage controlled switch.

3.19.3 Comments

N+ and *n–* are the positive and negative element nodes, respectively. *Nc+* and *nc–* are the controlling nodes. *Mname* is the model name. A switch is a resistor between *n+* and *n–*. The value of the resistor is determined by the state of the switch.

The resistance between *n+* and *n–* will be *RON* when the controlling voltage (between *nc+* and *nc–*) is above *VT + VH*. The resistance will be *ROFF* when the controlling voltage is below *VT - VH*. When the controlling voltage is between *VT - VH* and *VT + VH*, the resistance will retain its prior value.

You may specify `ON` or `OFF` to indicate the initial state of the switch when the controlling voltage is in the hysteresis region.

`RON` and `ROFF` must have finite positive values.

3.19.4 Model Parameters

`VT` = *x* Threshold voltage. (Default = 0.)

`VH` = *x* Hysteresis voltage. (Default = 0.)

`RON` = *x* On resistance. (Default = 1.)

`ROFF` = *x* Off resistance. (Default = 1e12)

3.20 T: Transmission Line

3.20.1 Syntax

T*xxxxxxx n1+ n1– n2+ n2–* {*args*}
`.TLIne` *xxxxxxx n1+ n1– n2+ n2–* {*args*}

3.20.2 Purpose

Lossless transmission line.

3.20.3 Comments

N1+ and *n1–* are the nodes at one end. *N2+* and *n2–* are the nodes at the other end.

The parameters `TD`, `Freq`, and `NL` determine the length of the line. Either `TD` or `Freq` and `NL` must be specified. If only `Freq` is specified, `NL` is assumed to be .25. The other will be calculated based on the one you specify. If you specify too much, `Freq` and `NL` dominate, and a warning is issued.

3.20.4 Element Parameters

`Z0` = *x* Characteristic impedance. (Default = 50.)

`TD` = *x* Time delay.

`Freq` = *x* Frequency for NL.

`NL` = *x* Number of wavelengths at *Freq*.

3.21 U: Logic Device

3.21.1 Syntax

U*xxxxxxx out gnd vdd enable in1 in2 ... family gatetype*

3.21.2 Purpose

Logic element for mixed or logic mode simulation.

3.21.3 Comments

A sample 2 input nand gate might be: `U102 5 0 34 34 2 3 cmos nand`. The input pins are connected to nodes 2 and 3. The output is at node 5. Node 34 is the power supply.

The logic element behaves differently depending on the options `analog`, `mixed`, or `digital`. You set one of these with the `options` command. `Analog` mode substitutes a subcircuit for the gate for full analog simulation. `Digital` mode simulates the gate as a digital device as in an event driven gate level logic simulator. `Mixed` mode applies heuristics to decide whether to use analog or digital for each gate.

In `analog` mode the logic (`U`) device is almost the same as a subcircuit (`X`). The subcircuit is user defined for each gate type used. A `.subckt` defines the analog equivalent of a logic element. The name of the subcircuit is made by concatenating the *family*, *gatetype*, and the number of inputs. For example, if the *family* is `cmos` and the *gatetype* is `nand` and it has two inputs, the name of the subcircuit is `cmosnand2`. So, the gate in the first paragraph becomes equivalent to: `X 5 0 34 34 2 3 cmosnand2`. You then need to

define the subcircuit using the standard `.subckt` notation. You can probe the internal elements the same as an ordinary subcircuit.

The `digital` mode uses simple boolean expressions to compute the output, just like a gate level logic simulator. In this case the output is computed by L(5) = not(L(2) and L(3)) where L(2) is the logic state at node 2. The simulator exploits latency so it will only compute the output if one of the inputs changes. The output actually changes after a delay, specified in the `.model` statement. There are no conversions between digital and analog where gates connect together. There will be an automatic conversion from analog to digital for any input that is driven by an analog device. There will be an automatic conversion from digital to analog for any output that drives an analog device. These conversions will only be done if they are needed. You can probe the analog value at any node. The probe will automatically request the conversion if it needs it. There is no internal subcircuit so it is an error to probe the internal elements.

The `mixed` mode is a combination of analog and digital modes on a gate by gate basis. Some gates will be analog. Some will be digital. This will change as the simulation runs based on the quality of the signals. You need to specify a `.subckt` as you do for the analog mode, but the simulator may not use it. You can usually not probe the elements inside the sibcircuit because they come and go.

3.21.4 Element Parameters

Family refers to the logic family `.model` statement.

Gatetype is the type of logic gate:

`AND`

`NAND`

`OR`

`NOR`

`XOR`

`INV`

3.21.5 Model Parameters

Parameters used in digital mode

`DElay` = x Propagation delay. (Seconds) (Default = 1e-9) The propagation delay of a simple gate when simulated in logic mode.

Parameters used in conversion both ways

`VMAx` = x Nominal logic 1. (Volts) (Default = 5.) The nominal value for a logic 1.

`VMIn` = x Nominal logic 0. (Volts) (Default = 0.) The nominal value for a logic 0.

`Unknown` = x Nominal logic unknown. (Volts) (Default = (vmax+vmin)/2) The output voltage for a logic unknown. In a real circuit, this voltage is unknown, but a simulator needs something, so here it is.

Digital to Analog conversion

`RIse` = x Rise time. (Seconds) (Default = delay / 2) The nominal rise time of a logic signal. This will be the rise time when a logic signal is converted to analog.

`FAll` = x Fall time. (Seconds) (Default = delay / 2) The nominal fall time of a logic signal. This will be the fall time when a logic signal is converted to analog.

`RS` = x Series resistance, strong. (Ohms) (Default = 100.) The resistance in series with the output when a logic gate drives analog circuitry.

`RW` = x Series resistance, weak. (Ohms) (Default = 1e9) The output resistance in a high impedance state.

Analog to Digital conversion

`THH` = x Threshold high. (Unitless) (Default = .75) The threshold for the input to cross from transition to high expressed as a fraction of the difference between high and low values. (Low = 0. High = 1.)

`THL` = x Threshold low. (Unitless) (Default = .25) The threshold for the input to cross from transition to low expressed as a fraction of the difference between high and low values. (Low = 0. High = 1.)

Mode decision parameters

`MR` = x Margin rising. (Unitless) (Default = 5) How much worse than nominal the analog input rise time can be and still be accepted as clean enough for logic simulation.

`MF` = x Margin falling. (Unitless) (Default = 5) How much worse than nominal the analog input fall time can be and still be accepted as clean enough for logic simulation.

`OVer` = x Overshoot limit. (Unitless) (Default = .1) How much overshoot can a signal have and still be accepted as clean enough for logic simulation, expressed as a fraction of the difference between high and low values. (Low = 0. High = 1.)

3.21.6 Probes

`V` Output voltage.

In this release, there are no probes available in AC analysis except for the internal elements. Internal elements in the analog model are available, but they come and go so they may be unreliable. More parameters will be added.

You can probe the logic value at any node. See the `print` command for details.

3.22 V: Independent Voltage Source

3.22.1 Syntax

V*xxxxxxx n+ n– value*
V*xxxxxxx n+ n– expression*
`.VSOurce` *label n+ n– expression*

3.22.2 Purpose

Independent voltage source.

3.22.3 Comments

N+ and *n–* are the positive and negative element nodes, respectively. *Value* is the voltage in Volts.

All of the SPICE time dependent functions (`pulse`, `sin`, `exp`, `pwl`, and `sffm` are supported. An additional function `generator` emulates a laboratory type function generator, for a more convenient signal input to the circuit.

3.23 W: Current Controlled Switch

3.23.1 Syntax

W*xxxxxxx n+ n– ce mname* {*ic*}
`.ISWitch` *label n+ n– ce mname* {*ic*}

3.23.2 Purpose

Current controlled switch.

3.23.3 Comments

N+ and *n–* are the positive and negative element nodes, respectively. *Ce* is the name of an element through which the controlling current flows. *Mname* is the model name. A switch is a resistor between *n+* and *n–*. The value of the resistor is determined by the state of the switch.

The resistance between *n+* and *n–* will be *RON* when the controlling current (through *ce*) is above *IT + IH*. The resistance will be *ROFF* when the controlling current is below *IT - IH*. When the controlling current is between *IT - IH* and *IT + IH*, the resistance will retain its prior value.

You may specify `ON` or `OFF` to indicate the initial state of the switch when the controlling current is in the hysteresis region.

`RON` and `ROFF` must have finite positive values.

The controlling element can be any simple two terminal element. Unlike SPICE, it does not need to be a voltage source.

3.23.4 Model Parameters

`IT` = x Threshold current. (Default = 0.)

IH = x Hysteresis current. (Default = 0.)

RON = x On resistance. (Default = 1.)

ROFF = x Off resistance. (Default = 1e12)

3.24 X: Subcircuit Call

3.24.1 Syntax

X*xxxxxxx n1* {*n2 n3 ...*} *subname*

3.24.2 Purpose

Subcircuit call

3.24.3 Comments

Subcircuits are used by specifying pseudo-elements beginning with X, followed by the connection nodes.

3.24.4 Probes

Vx Port (terminal node) voltage. x is which port to probe. 1 is the first node in the "X" statement, 2 is the second, and so on.

P Power. The sum of the power probes for all the internal elements.

PD Power dissipated. The total power dissipated as heat.

PS Power sourced. The total power generated.

In this release, there are no probes available in AC analysis except for the internal elements. More parameters will be added. Internal elements can be probed by concatenating the internal part label with the subcircuit label. R5.X7 is R5 inside X7.

3.25 Y: Admittance

3.25.1 Syntax

Y*xxxxxxx n+ n– value*
Y*xxxxxxx n+ n– expression*
.ADMittance *label n+ n– expression*

3.25.2 Purpose

Admittance, or general voltage controlled dissipative element.

3.25.3 Comments

N+ and *n–* are the positive and negative element nodes, respectively. *Value* is the admittance in Mhos.

The resistor (type R) differs from the admittance (type Y) in that the resistor is a current controlled element, and the conductance is a voltage controlled element, in addition to the obvious use of conductance ($1/R$) instead of resistance.

Chapter 4

Behavioral modeling

ACS behavioral modeling is in a state of transition, so this is subject to change in a future release.

Basically, all simple components can have a behavioral description, with syntax designed as an extension of the Spice time dependent sources. They are not necessarily physically realizeable. Some only work on particular types of analysis, or over a small range of values. Some can be used together, some cannot.

In general, all somple components are considered to have simple transformations. A function returns one parameter as a function of one other, as an extension of their linear behavior.

Linear behavior:

`Capacitor` $q = Cv$

`Inductor` $\phi = Li$

`Resistor` $v = Ir$

`Admittance` $i = Yv$

`VCVS` $v_o = Ev_i$

`VCCS` $i_o = Gv_i$

`CCVS` $v_o = Ei_i$

`CCCS` $i_o = Gi_i$

Sources are defined as functions of time:

`Voltage source` $v = f(t)$

`Current source` $i = f(t)$

For behavioral modeling / nonlinear values, replace the constant times input by an arbitrary function:

`Capacitor` $q = f(v)$

`Inductor` $\phi = f(i)$

`Resistor` $v = f(r)$

`Admittance` $i = f(v)$

`VCVS` $v_o = f(v_i)$

`VCCS` $i_o = f(v_i)$

`CCVS` $v_o = f(i_i)$

`CCCS` $i_o = f(i_i)$

Conditionals

`AC` AC analysis only.

`DC` DC/OP/Transient/Fourier analysis only

`DCOP` DC/OP analysis only.

`DCONLY` DC analysis only.

`DCTRAN` DC/OP/Transient/Fourier analysis only (same as DC)

`OP` OP analysis only.

`TRAN` Transient analysis only.

`ELSE` Anything not listed.

Functions

`COMPLEX` Complex (re, im) value.

`EXP` Spice Exp source. (time dependent value).

`GENERATOR` Value from Generator command.

`POLY` Polynomial (Spice style).

`POSY` Posynomial (Like poly, non-integer powers).

`PULSE` Spice Pulse source. (time dependent value).

`PWL` Piece-wise linear.

`SFFM` Spice Frequency Modulation (time dependent value).

`SIN` Spice Sin source. (time dependent value).

`TANH` Hyperbolic tangent xfer function.

4.1 Conditionals

ACS behavioral modeling conditionals are an extension of the "AC" and "DC" Spice source parameters.

The extensions ...

1. There are more choices, including an "else".
2. They apply to all elements (primitive components).
3. Each section can contain functions and options.

They are interpreted as an if, else-if, else statement. The first condition that is true applies.

The following are available:

`AC` AC analysis only.

`DC` DC/OP/Transient/Fourier analysis only

`DCOP` DC/OP analysis only.

`DCONLY` DC analysis only.

`DCTRAN` DC/OP/Transient/Fourier analysis only (same as DC)

`OP` OP analysis only.

`TRAN` Transient/Fourier analysis only.

`ELSE` Anything not listed.

4.1.1 Examples

`V12 1 0 AC 1 DC 3` This voltage source has a value of 1 for AC analysis, 3 for DC, OP, Transient, and Fourier analysis.

`R44 2 3 OP 1 ELSE 1g` This resistor has a value of 1 ohm for the "OP" analysis, 1 gig-ohm for anything else. This might be useful as the feedback resistor on an op-amp. Set it to 1 ohm to set the operating point, then 1 gig to measure its open loop characteristics, hiding the fact that the op-amp would probably saturate if it was really left open loop.

4.2 Functions

ACS behavioral modeling functions are an extension of the Spice source time dependent values.

4.2.1 The extensions

They apply to all elements (primitive components).

All accept either Spice compatible order dependent parameters, or easier keyword=value notation.

Some of the Hspice nonlinear functions are provided.

The syntax is identical for all supported components. This might force it to be a little different from Hspice, even where functionality is the same.

4.2.2 Fixed sources

Time dependent functions are voltage or current as a function of time. They are mostly Spice compatible, with extensions.

Nonlinear transfer functions use time as the independent variable. Some may not make sense, but they are there anyway.

4.2.3 Capacitors and inductors

Time dependent functions are capacitance or inductance as a function of time. They are voltage/current conserving, not charge/flux conserving.

Nonlinear transfer functions are charge or flux as a function of input (voltage or current). THIS IS

NOT COMPATIBLE WITH HSPICE. ACS will accept the HSPICE syntax, but it is interpreted different. Charge and flux are conserved, and can be probed.

4.2.4 Resistors and conductances

Time dependent functions are resistance or conductance as a function of time.

Nonlinear transfer functions are current or voltage as a function of input (voltage or current). Resistors define voltage as a function of current. Conductances define current as a function of voltage.

4.2.5 Controlled sources

Time dependent functions are gain (v/v, transconductance, etc) function of time.

Nonlinear transfer functions are output (voltage or current) as a function of input (voltage or current).

4.2.6 Available functions

`COMPLEX` Complex (re, im) value.

`EXP` Spice Exp source. (time dependent value).

`GENERATOR` Value from Generator command.

`POLY` Polynomial (Spice style).

`POSY` Posynomial (Like poly, non-integer powers).

`PULSE` Spice Pulse source. (time dependent value).

`PWL` Piece-wise linear.

`SFFM` Spice Frequency Modulation (time dependent value).

`SIN` Spice Sin source. (time dependent value).

`TANH` Hyperbolic tangent transfer function.

4.2.7 Parameters that apply to all functions

These parameters are available with all functions. Some may not make sense in some cases, but they are available anyway.

`Bandwidth` = x AC analysis bandwidth. (Default = infinity.) The transfer function is frequency dependent, with a 3 DB point at this frequency. There is frequency dependent phase shift ranging from 0 degrees at low frequencies to 90 degrees at high frequencies. The phase shift is 45 degrees at the specified frequency. AC ANALYSIS ONLY.

`Delay` = x AC analysis delay. (Default = 0.) The signal is delayed by x seconds, effectively by a frequency dependent phase shift. AC ANALYSIS ONLY.

`Phase` = x AC analysis phase. (Default = 0.) A fixed phase shift is applied. This is primarily intended for sources, but applies to all elements. AC ANALYSIS ONLY.

`IOffset` = x Input offset. (Default = 0.) A DC offset is added to the "input" of the element, before evaluating the function.

`OOffset` = x Output offset. (Default = 0.) A DC offset is added to the "output" of the element, after evaluating the function.

`Scale` = x Transfer function scale factor. (Default = 1.) The transfer function is multiplied by a constant.

`TNOM` = x Nominal temperature. (Default = .option TNOM) The nominal values apply at this temperature.

`TC1` = x First order temperature coefficient. (Default = 0.)

`TC2` = x Second order temperature coefficient. (Default = 0.)

`IC` = x Initial condition. An initial value, to force at time=0. The actual parameter applied depends on the component. (Capacitor voltage, inductor current. All others ignore it.) You must use the "UIC" option for it to be used.

Temperature adjustments and scaling use the following formula:

```
value *= _scale * (1 + _tc1*tempdiff
             + _tc2*tempdiff*tempdiff)
```

where `tempdiff` is `t - _tnom`.

4.3 COMPLEX: Complex value

4.3.1 Syntax

COMPLEX *realpart imaginarypart options*

4.3.2 Purpose

Complex component value, using a real and imaginary part. AC only.

4.3.3 Comments

Strictly, this adds no functionality over the polar option on any function, except notational convenience.

4.3.4 Example

`V12 2 0 complex 1,2` A voltage source with a value of 1 + j2 volts.

4.4 EXP: Exponential time dependent value

4.4.1 Syntax

EXP *args*
EXP *iv pv td1 tau1 td2 tau2 period*

4.4.2 Purpose

The component value is an exponential function of time.

4.4.3 Comments

For voltage and current sources, this is the same as the Spice EXP function, with some extensions.

The shape of the waveform is described by the following algorithm:

```
ev = _iv;
for (reltime=time; reltime>=0; reltime-=_period){
  if (reltime > _td1){
    ev += (_pv - _iv)
          * (1. - Exp(-(reltime-_td1)/_tau1));
  }
  if (reltime > _td2){
    ev += (_iv - _pv)
          * (1. - Exp(-(reltime-_td2)/_tau2));
  }
}
```

4.4.4 Parameters

`IV` = x Initial value. (required)

`PV` = x Pulsed value. (required)

`TD1` = x Rise time delay. (Default = 0.)

`TAU1` = x Rise time constant. (Default = 0.)

`TD2` = x Fall time delay. (Default = 0.)

`TAU2` = x Fall time constant. (Default = 0.)

`Period` = x Repeat period. (Default = infinity.)

4.5 GENERATOR: Signal Generator time dependent value

4.5.1 Syntax

GENERATOR *scale*

4.5.2 Purpose

The component "value" is dependent on a "signal generator", manipulated by the "generator" command.

4.5.3 Comments

For transient analysis, the "value" is determined by a signal generator, which is considered to be external to the circuit and part of the test bench. See the "generator" command for more information.

For AC analysis, the value here is the amplitude.

Strictly, all of the functionality and more is available through the Spice-like behavioral modeling functions, but this one provides a user interface closer to the function generator that an analog designer would use on a real bench. It is mainly used for interactive operation.

It also provides backward compatibility with predecessors to ACS, which used a different netlist format.

4.6 POLY: Polynomial nonlinear transfer function

4.6.1 Syntax

POLY *c0 c1 c2 c3 ...*
POLY *c0 c1 c2 c3 ... args*

4.6.2 Purpose

Defines a transfer function by a one dimensional polynomial.

4.6.3 Comments

This is similar to, but not exactly the same as, the HSPICE POLY(1).

For capacitors, this function defines *charge* as a function of voltage. For inductors, it defines *flux* as a function of current. This is not compatible with HSPICE. If you have the coefficients defining capacitance or inductance, prepending a "0" to the list will turn it into the correct form for ACS.

For controlled sources, it is compatible with HSPICE.

For fixed sources, it defines voltage or current as a polynomial function of time.

The transfer function is defined by:

```
out = c0 + (c1*in) + (c2*in^2) + ....
```

4.6.4 Parameters

MIN = *x* Minimum output value (clipping). (Default = -infinity.)

MAX = *x* Maximum output value (clipping). (Default = infinity)

ABS Absolute value, truth value. (Default = false). If set to true, the result will be always positive.

4.7 POSY: Polynomial with non-integer powers

4.7.1 Syntax

POSY *c1,p1 c2,p2 ...*
POSY *c1,p1 c2,p2 ... args*

4.7.2 Purpose

Defines a transfer function by a one dimensional "posynomial", like a polynomial, except that the powers are arbitrary, and usually non-integer.

4.7.3 Comments

There is no corresponding capability in any SPICE that I know of.

For capacitors, this function defines *charge* as a function of voltage. For inductors, it defines *flux* as a function of current.

For fixed sources, it defines voltage or current as a function of time.

Normal use of this function required positive input (voltage or current). The result is zero if the input is negative. Raising a negative number to a non-integer power would produce a complex result, which implies a non-causal result, which cannot be represented in a traditional transient analysis.

The transfer function is defined by:

```
if (in > 0){
  out = (c1*in^p1) + (c2*in^p2) + ....
}else{
  out = 0.
}
```

4.7.4 Parameters

MIN = *x* Minimum output value (clipping). (Default = -infinity.)

MAX = *x* Maximum output value (clipping). (Default = infinity)

ABS Absolute value, truth value. (Default = false). If set to true, the result will be always positive.

4.7.5 Example

`E1 2 0 1 0 posy 1 .5` The output of `E1` is the square root of its input.

4.8 PULSE: Pulsed time dependent value

4.8.1 Syntax

PULSE *args*
PULSE *iv pv delay rise fall width period*

4.8.2 Purpose

The component value is a pulsed function of time.

4.8.3 Comments

For voltage and current sources, this is the same as the Spice PULSE function, with some extensions.

The shape of a single pulse is described by the following algorithm:

```
if (time > _delay+_rise+_width+_fall){
  // past pulse
  ev = _iv;
}else if (time > _delay+_rise+_width){
  // falling
  interp=(time-(_delay+_rise+_width))/_fall;
  ev = _pv + interp * (_iv - _pv);
}else if (time > _delay+_rise){
  // pulsed value
  ev = _pv;
}else if (time > _delay){
  // rising
  interp = (time - _delay) / _rise;
  ev = _iv + interp * (_pv - _iv);
}else{
  // initial value
  ev = _iv;
}
```

4.8.4 Parameters

IV = x Initial value. (required)

PV = x Pulsed value. (required)

DELAY = x Rise time delay, seconds. (Default = 0.)

RISE = x Rise time, seconds. (Default = 0.)

FALL = x Fall time, seconds. (Default = 0.)

WIDTH = x Pulse width, seconds. (Default = 0.)

PERIOD = x Repeat period, seconds. (Default = infinity.)

4.9 PWL: Piecewise linear function

4.9.1 Syntax

PWL *x1,y1 x2,y2 ...*

4.9.2 Purpose

Defines a piecewise linear transfer function or time dependent value.

4.9.3 Comments

This is similar to, but not exactly the same as, the Berkeley SPICE PWL for fixed sources, and the H-SPICE PWL for controlled sources..

For capacitors, this function defines *charge* as a function of voltage. For inductors, it defines *flux* as a function of current. This is not compatible with HSPICE.

For fixed sources, it defines voltage or current as a function of time.

The values of x must be in increasing order.

Outside the specified range, the behavior depends on the type of element. For fixed sources, the output (voltage or current) is constant at the end value. This is compatible with SPICE. For other types, the last segment is extended linearly. If you want it to flatten, specify an extra point so the slope of the last segment is flat.

4.9.4 Parameters

There are no additional parameters, beyond those that apply to all.

4.9.5 Example

`C1 2 0 pwl -5,-5u 0,0 1,1u 4,2u 5,2u` This "capacitor" stores 5 microcoulombs at -5 volts (negative, corresponding to the negative voltage, as expected. The charge varies linearly to 0 at 0 volts, acting like a 1 microfarad capacitor. (C = dq/dv). This continues to 1 volt. The

0,0 point could have been left out. The charge increases only to 2 microcoulombs at 4 volts, for an incremental capacitance of 1u/3 or .3333 microfarads. The same charge at 5 volts indicates that it saturates at 2 microcoulombs. For negative voltages, the slope continues.

4.10 SFFM: Frequency Modulation time dependent value

4.10.1 Syntax

SFFM *args*
SFFM *offset amplitude carrier modindex signal*

4.10.2 Purpose

The component value is a sinusoid, frequency modulated by another sinusoid.

4.10.3 Comments

For voltage and current sources, this is the same as the Spice SFFM function, with some extensions.

The shape of the waveform is described by the following equations:

```
mod = (_modindex * sin(2*PI*_signal*time));
ev = _offset + _amplitude
        * sin(2*PI*_carrier*time + mod);
```

4.10.4 Parameters

Offset = *x* Output offset. (Default = 0.)

Amplitude = *x* Amplitude. (Default = 1.)

Carrier = *x* Carrier frequency, Hz. (required)

Modindex = *x* Modulation index. (required)

Signal = *x* Signal frequency. (required)

4.11 SIN: Sinusoidal time dependent value

4.11.1 Syntax

SIN *args*
SIN *offset amplitude frequency delay damping*

4.11.2 Purpose

The component value is a sinusoidal function of time, with optional exponential decay.

4.11.3 Comments

For voltage and current sources, this is the same as the Spice SIN function, with some extensions.

It generates either a steady sinusoid, or a damped sinusoid.

If *delay* and *damping* are both zero, you get a steady sine wave at the specified *frequency*. Otherwise, you get a damped pulsed sine wave, starting after *delay* and damping out with a time constant of 1/*damping*.

The shape of the waveform is described by the following algorithm:

```
reltime = time - _delay
if (reltime > 0.){
  ev = _amplitude * sin(2*PI*_freq*reltime);
  if (_damping != 0.){
    ev *= exp(-reltime*_damping);
  }
  ev += _offset;
}else{
  ev = _offset;
}
```

4.11.4 Parameters

Offset = *x* DC offset. (Default = 0.)

Amplitude = *x* Peak amplitude. (Default = 1.)

Frequency = *x* Frequency, Hz. (required)

Delay = *x* Turn on delay, seconds. (Default = 0.)

Damping = *x* Damping factor, 1/seconds. (Default = 0.)

4.12 TANH: Hyperbolic tangent transfer function

4.12.1 Syntax

TANH *gain limit*
TANH *args*

4.12.2 Purpose

Defines a hyperbolic tangent, or soft limiting, transfer function.

4.12.3 Comments

There is no corresponding capability in any SPICE that I know of, but you can get close with POLY.

For capacitors, this function defines *charge* as a function of voltage. For inductors, it defines *flux* as a function of current.

For fixed sources, it defines voltage or current as a function of time, which is probably not useful.

This function describes a hyperbolic tangent transfer function similar to what you get with a single stage push-pull amplifier, or a simple CMOS inverter acting as an amplifier.

4.12.4 Parameters

GAIN = x The small signal gain at 0 bias. (Required)

LIMIT = x Maximum output value (soft clipping). (Required)

4.12.5 Example

```
E1 2 0 1 0 tanh gain=-10 limit=2 ioffset=2.5 ooffset=2.5
```

This gain block has a small signal gain of -10. The input is centered around 2.5 volts. The output is also centered at 2.5 volts. It "clips" softly at 2 volts above and below the output center, or at .5 volts $(2.5 - 2)$ and 4.5 volts $(2.5 + 2)$.

Chapter 5

Installation

Most of the development of ACS was done on a PC running Linux. I have also compiled it successfully on several other systems, listed at the end of this file. Other users have ported ACS to several other systems. Some of the files are included in the distribution. They may not have been tested in the latest release. It should compile with any "standard" C++ compiler. It should produce no warnings when compiled with the switches in the supplied makefiles and g++, except those due to the system supplied header files being defective. It requires templates, but not exceptions.

All source files are in the src directory. I use subdirectories for the .o files each supported machine. This makes it possible to install it on several different machines all sharing the same file system.

To avoid maintaining multiple versions of Makefiles, I have broken them up to parts that must be concatenated: Make1.*, Make2.*, Make3.*. In general, to make a Makefile for your system, cat one of each. See the Makefile for details. I have automated this for some systems. Just "make your-machine", if it is one that is supported. In some cases, the Makefile will compile both a "release" and "debug" version. In these cases, type "make your-machine-release" or "make your-machine-debug" depending on which you want. This will make the appropriate Makefile, cd to where the .o's go and run make from there. For porting information for specific machines, read its "Make2.*" file.

I assume that make will follow "VPATH" to find the sources. This system makes it possible to manage several platforms on a single file system which may be NFS mounted to all the supported machines. If your make does not support VPATH, there are three options. The preferred method on unix based systems is to cd to where the .o's go and type "ln -s ../*.cc ../*.h .". This will set up links so the Makefiles will work as intended. In some cases we have set up the Makefile to do this automatically. The second method, which may be needed on systems like MS-DOS that don't have symbolic links is to copy the .c and .h files to satisfy make. The third option, where you have only one computer, is to move the machine specific Makefile to the src directory and run make from there.

If you have g++ on a unix type system that is not directly supported, try to compile it by just typing "make". In most cases this will do it, but you may get a few warnings. If it doesn't work, look in the file md.h for hints. Just plain "make" will build a development version with additional debugging enabled. This results in a significant speed penalty.

Then make the installation version, select the machine you have from the make file and make that. The machine specific versions will build in their own directory, have debugging code disabled, and options are set for best speed. The general purpose "make g++" builds a version that is optimized as much as it can be in the general case.

If you have a cfront-type compiler, called "CC", and your system is not directly supported, try it first by typing "make CC". Again, you may get a few warnings but it should work. Look in the file md.h for hints, if it doesn't work, or if the warnings look serious.

Since C++ is an evolving language, there are some known portability problems:

bool The C++ language includes a type "bool", which is not implemented in older compiler-

s. By defining BAD_BOOL creates the "bool" type, which must be done in a roundabout way because the boolean operators may return int, which in some cases cannot be assigned to bool.

const C++ uses an abstract notion of constant, meaning that the external appearance of an object declared const must not change, but there can be internal changes like reference counters. The keyword "mutable" means that a member variable can change even if it is declared const. As a work around, ACS uses CONST, which is either defined to nothing or const. Defining NO_ABSTRACT_CONST defines out the CONST, making it work on older compilers. A related problem is that the header files supplied with some compilers do not implement const correctly.

complex The evolving standard shows complex to be a template class, so instead of having a type "complex", there is "complex<double>", "complex<float>", and so on. Older compilers have only "complex". The compiler should automatically define __STD_COMPLEX to indicate that it has the template, so selecting the proper mode should be automatic.

templates There are three common ways to instantiate templates in common use. Unfortunately, they are incompatible and none of the methods are available in all compilers. ACS requires templates, so will not work with many older compilers.

Link time The entire program is compiled and linked without templates, resulting in some unresolved externals. The files defining the templates are compiled again to fill the need. This is the preferred way, if you have it. It is supported by CFRONT derivatives such as the Sun CC compiler. Define LINK_TEMPLATES to force it. This is the default, unless you are using the GNU compiler.

Compile time All parts of templates must be compiled as if in-line, requiring all code to be in the .h file, or included by the .h file. Header files include .cc files. The duplicates are supposed to be thrown away by the linker. This is the only style supported by Borland 3.1 or 4.0. It is supported inefficiently by the GNU compiler starting at version 2.6. Define COMPILE_TEMPLATES (or ComTemP) to force it.

manual Templates must be instantiated manually. This is the preferred way for the GNU compiler. It is not supported by CFRONT or Borland. Define MANUAL_TEMPLATES to force it.

The second inconsistency with templates, is what type conversions are allowed. Some compilers require an exact match. Some will make trivial conversions, such as int to const int. If yours has a problem, define PEDANTIC_TEMPLATES (or PedTemP). Defining PEDANTIC_TEMPLATES when it is not needed may produce duplicates, so it MUST be one way or the other,

missing files or functions Another cause of a port to fail is missing header files or missing function prototypes. Sometimes missing functions can be a problem. The solution to these problems is to supply what is missing. The "md_*" files exist for this purpose. You should make a copy of the appropriate Make2.___ file, patch it to define something to identify the system, then patch the md_(whatever).h and md_(whatever).cc as appropriate. You should not use any #ifdef's except in these file.

bad header files In some cases, the header files that come with the system or compiler are defective and generate warnings without anything wrong with the program being compiled. This slips by in the distribution because most developers compile with warnings off. Usually, these can be ignored.

If a port doesn't work, probably there is a missing header file, prototype, or function. You need to supply what is missing. Suppose you have a "foobiac" computer. You should make a new file "Make2.foobiac" that defines the compiler switches. In CFLAGS, you should define "FOOBIAC" to select your patches. You should change "Makefile" to

make the directory "FOOBIAC" for the .o files and the special "Makefile". You should also add a few lines so when you type "make foobiac" in the "src" directory it builds the special "Makefile" then does (cd FOOBIAC; make -k) to make the program. Then you should edit the md_unix.h file to make the appropriate includes and prototypes for your system. Look at the files to see how we handle the other systems. If you do a port please share your patches so I can add it to the distribution.

If you have a non-unix system you may also need to change "md.cc" and "md.h" and make some new files "md_foobiac.cc" and "md_foobiac.h". Look at the files for other systems for a guide to what should be there. How you handle the "makefile" will depend on the tools you have.

Some files starting with "plot" contain plotting drivers are may also need customization if you want a graphic display. They are all essentially non-working, but plotibm does work for most PC video cards. If all you want are ASCII plots the files should be suitable as they are.

There should be NO non-portable code anywhere but the md_* files and plot files. The use of #ifdef to patch portability problems should be restricted to the md_* and plot files.

Chapter 6

Technical Notes

6.1 Transient analysis

6.1.1 The "CPOLY" and "FPOLY" classes

Before beginning a discussion of the evaluation and stamp methods, it is necessary to understand the "CPOLY" and "FPOLY" classes.

These classes represent polynomials. At present, only the first order versions are used, but consider that they could be extended to any order.

When evaluating a function $f(x)$, there are several possible representations for the result. The "CPOLY" and "FPOLY" represent two of them.

The "CPOLY" classes represent the result in a traditional polynomial form. Consider a series of terms, c0, c1, c2, ... These represent the coefficients of a Taylor series of the function expanded about x. Thus $f(x) = c_0 + c_1x + c_2x^2 + c_3x^3 + ...$ In most cases, only the c0 and c1 terms are used, hence the "CPOLY1" class.

The other "FPOLY" classes represent the same polynomial with a different view. Again, consider a series of terms, f0, f1, f2, ... This time the terms represent the function evaluated at x and its derivatives. Therefore, f0 is $f(x)$, f1 is the first derivative, f2 is the second derivative, and so on. Again, in most cases, only the f0 and f1 terms are used, hence the "FPOLY1" class.

Both of these are equivalent in the sense that they represent the same data, and there are functions (constructors) that convert between them. The "FPOLY" form is usually most convenient for function evaluation used in behavioral modeling and device modeling. The "CPOLY" form is most suitable for stamping into the admittance matrix and current vector for the final solution.

6.1.2 The basic solution algorithm

In simplified form, the algorithm looks like this ...
before doing anything ....

```
expand()
precalc()
```

on issuing the "tran" command ..

```
tr_begin() // get ready
for (each time step) {
  tr_advance() // precalculate and propagate
  for (each iteration) {
    tr_queue_eval() // decide which models need evaluat
    do_tr() // evaluate models
    tr_load() // build the matrix of equations
    solve the resulting system of equations
  }
  if (converged) {
    tr_review() // how are we doing? suggest time step
  }
  if (no problems) {
    tr_accept() // postcalculate and accept data
  }
}
```

The functions referred to above are actually loops that call that function for all devices in the circuit.

For all of them, it is possible that they may not be called. If there is evidence that the result will not change from the last time it was called, it probably will not be called. Since this algorithm is not perfect, it is possible that any particular function may be

called twice, so they are written so calling more than once is equivalent to calling once.

expand

The *expand* functions expand subcircuits and models, as needed. Unlike Spice, it does not flatten the circuit. It allocates space for the additional storage, attaches models, and related tasks. It does not compute any values. It is called once after reading the circuit, and possibly later when the topology of the circuit is changed.

Most elements do not have expand functions. Most advanced components do.

Expanding a subcircuit makes a copy of it, and remaps the nodes. Most components use a shallow copy. That is, if something is attached through a pointer, the value of the pointer is copied, not the attachment. Commons are never copied when the owner components are copied.

It is ok to expand a component more than once. Either it frees then re-expands, or it keeps what it can and checks to make sure it is correct.

precalc

The *precalc* functions attempt to pre-calculate anything that will remain constant during a simulation run. This includes size dependent transistor parameters and the stamp values for linear elements.

The actual evaluation of constant linear elements is done here. For nonlinear elements, it computes a first guess.

dc_begin, tr_begin, tr_restore

These functions are called once on issuing a simulation command. The *dc_begin* functions are called on starting a DC or OP anaylsis. The *tr_begin* functions are called on starting a transient analysis from time = 0, or the first time. The *tr_restore* functions are called on starting a transient analysis in such a way that the analysis continues from where a previous transient analysis left off.

The purpose is to make sure that the initial guesses and numbers for prior iterations that don't exist are properly set up. For linear elements, the values are set up here and are not computed later.

dc_advance, tr_advance

These functions are called before beginning a new time or voltage step.

For basic storage elements like capacitors, they store the data from the previous step. They may also attempt to predict a new value, in hopes of speeding up the real solution.

For delay elements like logic devices and transmission lines, this function does the real work. It takes previous results and applies them, generating data that will be later loaded into the matrix.

tr_needs_eval

This function returns true if the component needs to be evaluated on this iteration. It should return false if it has already been queued, but some do not do this.

tr_queue_eval

This function queues the component to be evaluated, if it needs it. If *tr_queue_eval* is not called, it will not be evaluated.

do_tr

In most cases, the *do_tr* functions do the real work, or call the *tr_eval* function to do it. It evaluates the model, checks convergence, and queues it for loading. Calling this function more than once on an iteration is harmless, except for the waste of time.

Usually, it calculates the function and derivative. It may also do integration, interpolation, iteration, or whatever is required. The result is a set of values ready to stamp into the admittance matrix and current vector.

tr_load

This function gives the appearance of loading the admittance matrix and current vector with the values calculated in *do_tr*.

Actually, it does much more. In most cases, it actually loads a correction factor, assuming the old values are already loaded. To do this, it keeps track of what values are actually loaded. Whether it loads a correction or the actual value is determined first by the option *incmode*, then by status information about

the solution. If it is suspected that correcting would cause too much roundoff error, it loads the actual value. The decision of whether to do a full load or an update is global.

In addition, it may apply damping in hopes of improving convergence. This means to load a value somewhere between the new and old values, in effect taking a partial step. The decision to damp is semi-global. Groups of elements are adjusted together.

The actual loading is done by one or more of a small group of general functions, depending on whether the element is active, passive, poly, or a source. Only certain patterns can be stamped. Complex devices use a combination of these patterns.

WARNING to model developers: DO NOT stamp the matrix directly!

tr_review

The *tr_review* function checks errors and signal conditions after a time step has converged. It makes entries into the event queue, makes mode decisions for mixed-mode simulation, and evaluates time step dependent errors. It returns an approximate time that the element wants for the next step. The actual next time step will probably be sooner than the value returned.

tr_accept

This function is called after the solution at a time step has been accepted. For most devices, it does nothing. For devices having storage and delayed propagation, it evaluates what signal will be propagated. For a transmission line, it calculates and sends on the reflections.

tr_unload

This function removes the component from the matrix, possibly by subtracting off what was loaded. Usually, it sets the current values to 0 and calls *tr_load*.

6.1.3 Step control

The basic algorithm

The basis of it is in the files "s_tr_swp.cc" and "s_tr_rev.cc".

The function TRANSIENT::review sets two variables: "approxtime" and "control".

The variable "approxtime" is a suggestion of what the next time should be. Note that this is a time, not a difference. Also note that the simulator may override this suggestion. Another "control" is an enum that shows how the time was selected. You can probe control(0) to find this code, or control(1) to see how many steps (not iterations) it calculated internally.

This time may be in the future, past, or again at the present time, depending on conditions. A time in the future means all is well, and the simulation can proceed as expected. A time in the past indicates something is wrong, such as convergence failure, excessive truncation error, or a missed event. In this case, the step is rejected, and time backed up. A repeat at the present time usually means a latency check failed. A portion of the circuit that was thought to be latent was found to be active. This usually indicates a model problem.

First, it attempts to suggest a time "rtime" based on iteration count and options.

There are several "options" that control the stepping:

- iterations > itl4 ... reduce by option "trstepshrink".
- iterations > itl3 ... suggest the same step as last time.
- else (iterations <= itl3) ... increase step size. Try the max as per userstepsize/skip limit to larger of (rdt*trstepgrow) where "rdt" is the old "review" estimate or (oldstep*trstepgrow) where oldstep is what was actually used last time and trstepgrow is an option, from the options command.

Second it makes another suggestion "tetime" based on truncation error, etc. It does this by calling the "review" function for all components, and taking the minimum. Any component can suggest a time for its next evaluation with its review function. Most

components return a very large number, letting the capacitors and inductors dominate, but it is not required for it to be so. This time should be in the future, but errors could produce a time in the past.

Then, the earliest time of the above two methods is selected. A time in the past means to reject the most recent time step and back up, but note that this time is only a suggestion that may not be used.

The function "TRANSIENT::sweep" essentially processes the loop "for (first(); notpastend; next())". The function "TRANSIENT::next()" actually advances (hopefully) to the next step. It may go backwards.

The actual time step depends on the suggestion by the review function (approxtime), the event queue (which includes what Spice calls "breakpoints"), the user step size (nexttick), and some tricks to minimize changes.

Some considerations ...

- Changing the step size is an expensive operation, because it usually forces a full LU decomposition and matrix reload. If the step can be kept constant, changes are limited to the right-side, eliminating the need for the full evaluation and LU.

- The simulator will place a time step exactly at any step for which the user has requested output, or Fourier analysis needs a point, or at any event from the event queue.

So, here it is ...

Assume we want it at the time the user requested. If the event queue says to do it sooner, take it, else take the user time. Note that this time is needed exactly, either now or later. If the "approxtime" is sooner than the exact time, inject a time step as follows... if the time step is less than half of the time to when an exact time is needed, take the approxtime, else take half of the exact interval, in hopes that the next step will use up the other half.

After that, there are some checks ....

"Very backward time step" means that the suggested new step is earlier than the PREVIOUS step, meaning that both the current step and its predecessor are rejected, thus it should back up two steps. Since ACS can back up only one step, it rejects the most recent step and tries again at the minimum step size. This usually means there is a bug in the software.

"Backwards time step" means to reject the most recent step, but the one before that is ok. It will reject the step and try again at the smaller interval. This happens fairly often, usually due to slow convergence.

"Zero time step" means that the new time is the same as the previous time, which usually means there is a bug in the software. Something is requesting a re-evaluation at the same time.

The combination of "zero time step" and "very backward time step" means that the re-evaluation didn't work.

Now, accept the new time and proceed.

The "review" function

Every component can have a "review" function, in which it can determine whether to accept or reject the solution. It will accept by suggesting a time in the future, or reject by suggesting a time in the past. It returns the suggested time. It can call new_event to request an exact time.

For capacitors and inductors, the review function attempts to estimate truncation error using a divided difference method, and it suggests a time for the next solution that will result in meeting the error requirement. Occasionally, it will discover that the step just computed fails to meet the requirement, so it will reject it.

Truncation error is related to the third derivative of charge or flux. Since current is the first derivative of charge, it would seem that second derivative of current should produce the same results faster. In practice, the current based method tends to estimate high leading to smaller steps, and the charge based method tends to estimate low, leading to larger steps. The conservative approach would suggest using the current based method, but that sometimes led to unreasonably small steps ans slow simulations, so I chose (as Spice did) the other method. Either method is ok when the step size used is close to being reasonable, but when the trial step is unreasonably large, either approach gives a very poor estimate. Taking a step much too small will make the simulator run much slower, as it takes many steps, then the step size is allowed to grow slowly. This is slower both because of the many unnecessary steps, and because

of many adjustments. Taking a step that is much too large will result in a choice that is better than the first trial, which will make a better estimate and be rejected. It is rare to get more than one rejection based on truncation error.

Conclusion

ACS will usually do more time steps than Spice will, due to 2 factors. ACS will force calculations at print points and fourier points, and can reject a bad step. It is usually a little more, but could be as much as twice as many steps.

6.2 Data Structures

6.2.1 Parts list

Main parts list

The primary data storage is in a list of "cards". A card is anything that can appear in a net list. Cards live here, primarily, but there are some other auxilary lists that also contain pointers to cards.

The list stores pointers, rather than actual objects, because there are many types of cards. All are derived from the "card", through several levels of inheritance.

Usually, they are stored in the order they are read from the file, except for subcircuits, which are stored in separate lists to preserve the hierarchy.

As of release 0.24, the main list is in static storage, so there can be only one. This will change. New cards can be inserted anywhere in the list, but usually they are inserted at the end. The mechanism for marking the location is a hybrid of STL and a 15 year old pointer scheme, which will also change someday.

The "Common" and "Eval" classes

The "common" serves two distinct purposes. The first is to share storage for similar devices. The second is to attach "evaluators" to otherwise simple components for special behavior.

Most circuits have many identical elements. The "common" enables them to share storage. One "common" can be attached to many devices. When a new device is created, even if it is parses separately, an attempt is made to find an appropriate device to share with.

Simple elements like resistors and capacitors can have "evaluators" attached as commons. These evaluators calculate a function and its derivative, and return it in a standard form. Some evaluators are used internally, such as in the diode and mosfet models. Some are used explicitly, such as in behavioral modeling.

6.3 Performance

This section gives some notes on some of the performance issues in ACS. It is not intended to be complete or well organized.

6.3.1 Virtual functions

There is a question of the impact on speed from the use of virtual functions. The experiment used here is to use the circuit `eq4-2305.ckt` from the examples directory, and try several modified versions of the program. I used a 100 point dc sweep, a version between 0.20 and 0.21, and made several modifications for testing purposes. I chose this circuit because it has little to mask the effect, and therefore is sort of a worst case.

I added an int `foo` to the element class. I made the function `il_trload_source` call a virtual function `virtual_test` and stored the result. The local version body has a print call, which should not show, to make sure it calls the other. These functions simply return a constant, determined by which version of the function is called. Run time is compared, with and without this.

With 1 virtual function call (included in load)

	user	sys	total
evaluate	13.45	0.11	13.56
load	13.40	0.06	13.47
lu	1.91	0.09	2.00
back	22.35	0.27	22.61
review	0.00	0.00	0.00
output	0.11	0.11	0.22
overhead	0.23	0.19	0.42
total	51.45	0.83	52.28

With 10 virtual function calls (included in load)

	user	sys	total
evaluate	13.47	0.09	13.57
load	24.69	0.17	24.87
lu	2.09	0.02	2.11
back	22.17	0.35	22.51
review	0.00	0.00	0.00
output	0.14	0.11	0.25
overhead	0.25	0.25	0.50
total	62.82	0.99	63.81

No extra function calls (included in load)

	user	sys	total
evaluate	13.41	0.09	13.50
load	11.75	0.05	11.79
lu	2.04	0.03	2.07
back	22.51	0.33	22.84
review	0.00	0.00	0.00
output	0.08	0.11	0.19
overhead	0.31	0.25	0.56
total	50.10	0.86	50.96

My conclusion is that in this context, even a single virtual function call is significant (10-15% of the load time), but not so significant as to prohibit their use. The load loop here calls one virtual function inside a loop. The virtual function calls an ordinary member function. Therefore, about 30% of the load time is function call overhead.

The impact should be less significant for complex models like transistors because the calculation time is much higher and would serve to hide this better.

Spice uses a different architecture, where a single function evaluates and loads all elements of a given type. This avoids these two calls.

6.3.2 Inline functions

For this test, `il_trload_source` is not inline. Contrast to "No extra function calls" and "1 virtual function" above, in which this function is inline.

	user	sys	total
evaluate	13.44	0.15	13.60
load	13.85	0.14	13.99
lu	1.73	0.02	1.75
back	22.89	0.35	23.24
review	0.00	0.00	0.00
overhead	0.45	0.17	0.63
total	52.50	0.94	53.44

This shows (crudely) that the overhead of an ordinary private member function call (called from another member function in the same class) is significant here. The cost of a virtual function call is comparable to the cost of an ordinary private member function call.